Tyndall National Institute
Institiúid Náisiúnta

180nm CMOS Buck-Boost Converter with Mixed Signal Control for 1uW to 100mW Power Conversion

EnerHarv 2022

6th April 2022

Séamus O'Driscoll

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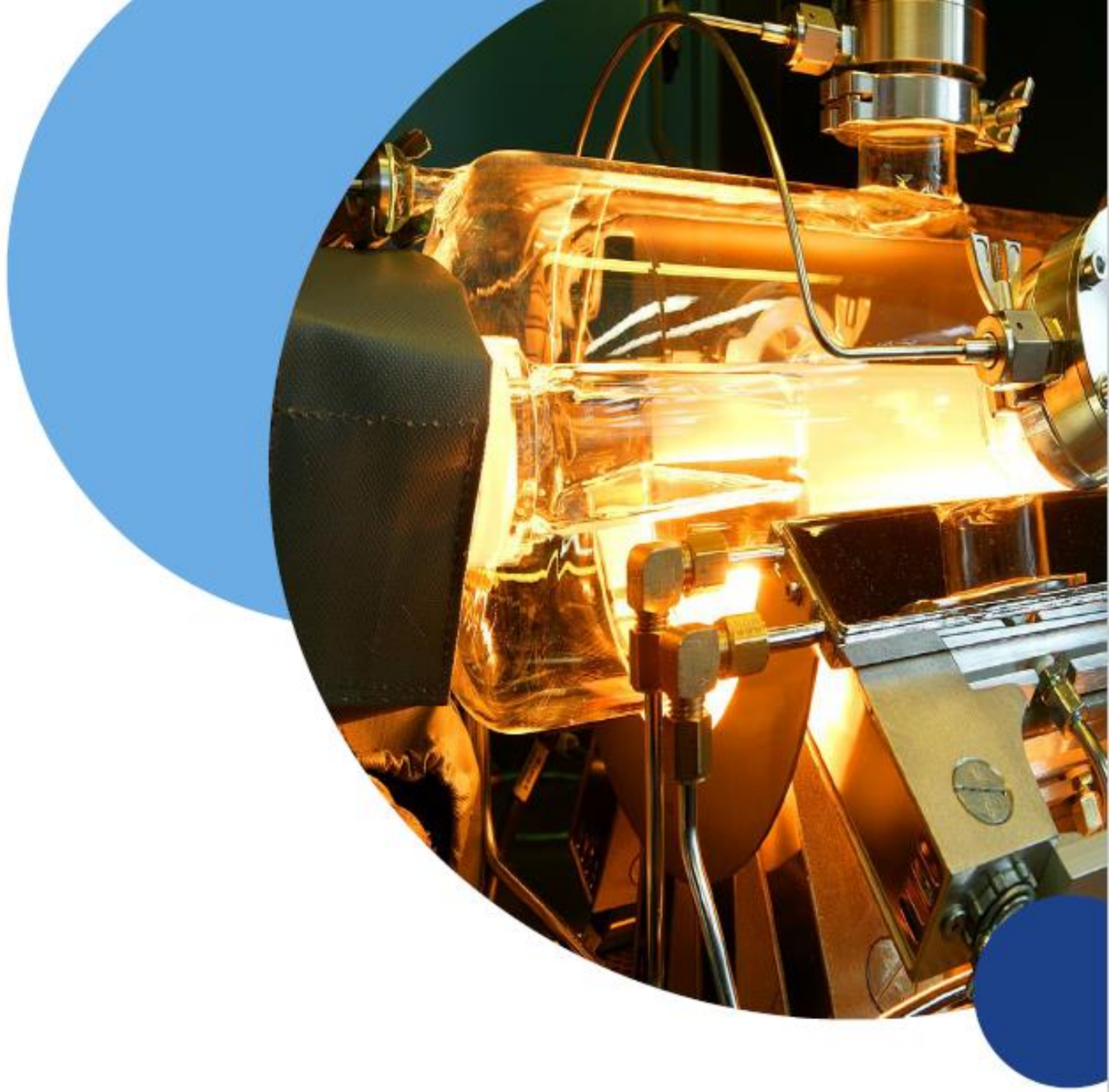
www.mcci.ie; www.tyndall.ie



UCC University College Cork, Ireland Coláiste na hOllscoile Corcaigh

MCCI SOLVE THE IMPOSSIBLE

Rialtas na hÉireann Government of Ireland | Tionscadal Éireann Project Ireland 2040

Ireland's European Structural and Investment Funds Programmes 2014-2020 Co-funded by the Irish Government and the European Union

European Union European Structural and Investment Funds

Powering the trillion ultra low power sensor nodes

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- Multiple dynamic intermittent sources
- Large dynamic ranges in source and load powers, 10^5 +
- Complex Power Systems
  - *Power/Energy Centric* Systems;
- Large Variety of Variable Ambient Environments
- Source Power Transducer Efficacy Improvements
  - Power Factor Correction, Synchronous Charge Extraction
- Advanced Features
  - Gas-Gauge, MPPT, Condition Monitoring, System Optimisation

PLATFORM VISION

- Highest efficiency from < 1 µW
- Multiple inputs, outputs and power flow directions
- DC, AC Sources from 30 mV to 100s’ V
- SPI Digitally Configurable
- Flexible Architecture
- Asynchronously triggerable functionality blocks
- **Solution by State Machine design -> Register Config -> + Micro Code**
- Support the SoC with Transducer, Storage and Load Interface
- Based on the premise that energy efficient digital control is feasible for advanced features – MPPT, Energy and Condition Metrology

Platform Approach: Power and Energy

Designing for On-State – *Energy Per*

- *On state* Quiescent power
- Optimum Energy transfer per switching cycle
- Energy per timed second
- Energy per PFM modulator cycle
- Energy per control sample – dynamic bandwidth, as required
- Energy per function

BURST MODE

Designing for Off-State – leakage power minimisation

- Minimum Power during Burst Spaces
- Low sleep mode – with timed wake or analog event driven wake

Duty Cycling – asynchronously triggered circuits – rapid on-off - functionality on demand

- Dynamic Comparators, Oscillators, References, Amplifiers, ADC, DACs

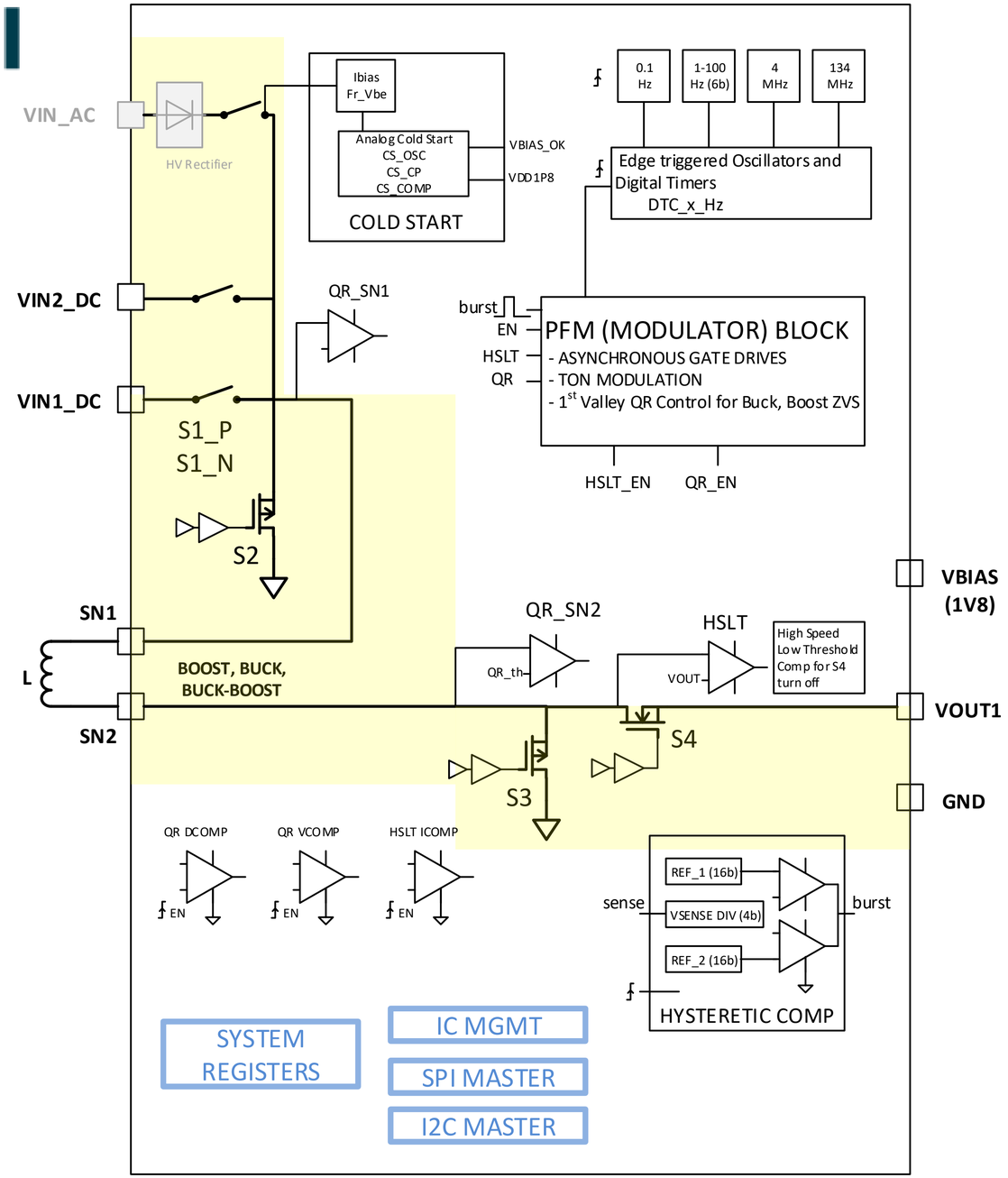
IC Process

Process: XFAB 180nm, LP CMOS, BCD, SOI

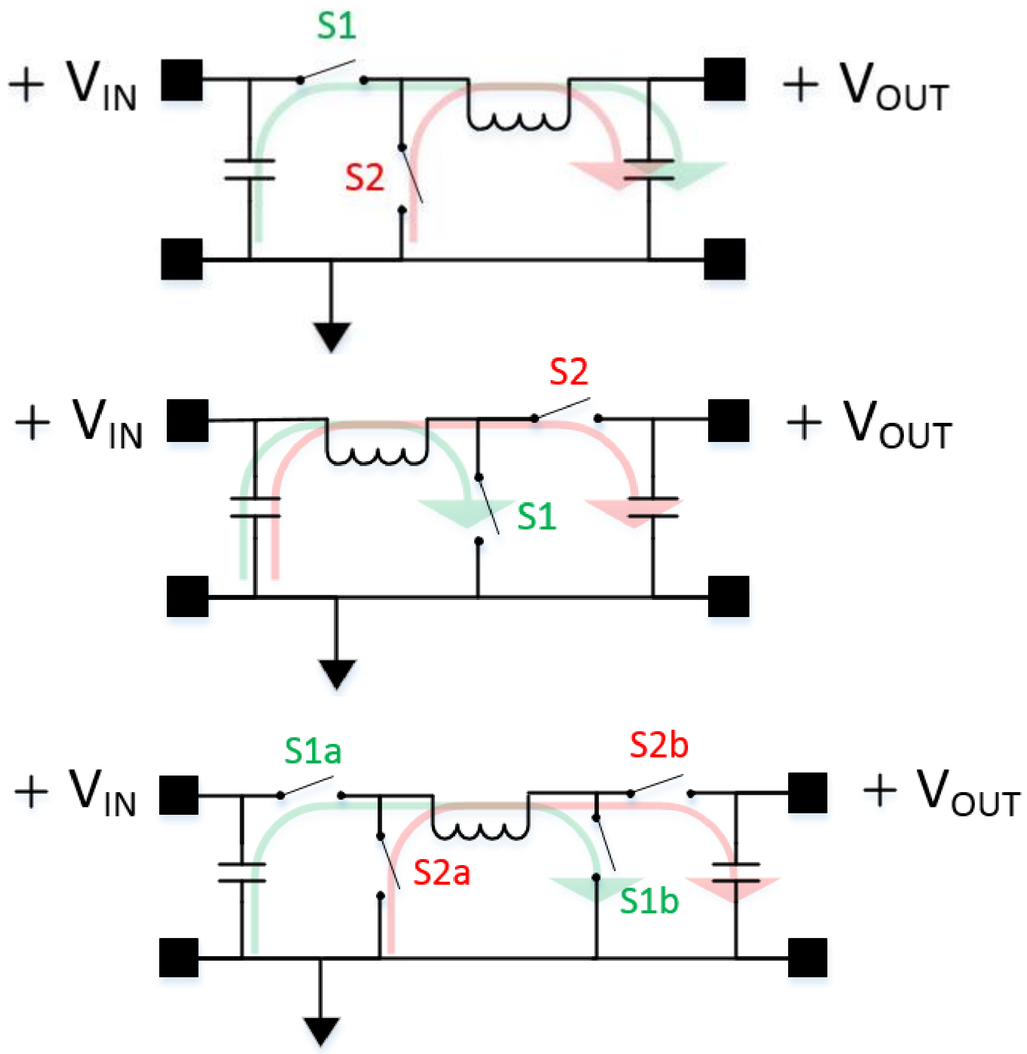
- Automotive, Medical and -40C-175C
- Practically 50kgates/mm^2
- 1.8 – 200 V switches

- XFAB have a range of MEMs Processes
  - 8 um Cu
  - Electrochemical cell films

- Micro Transfer Printing of 10 um chiplets
- with X-Celeprint (www.X-Celeprint.com) (hosted at Tyndall)



Switch Mode Inductor Topologies



Buck

$V_{IN} > V_{OUT}$

Boost

$V_{OUT} > V_{IN}$

Buck-Boost

$V_{OUT} <,> V_{IN}$

Inductors are beautifully voltage compliant

Buck or Boost is more efficient than Buck-Boost

The Buck-Boost can cater for multiple and varied interleaved sources and outputs

Inductors are large when looking for small Δi

Parking the challenge of topology change and inductor integration

Post Layout (PEX) Simulated Performance

PEX Simulations IC (M2a)

Boost Mode 1V5 to 3V

PFM_BSTSR_TST1 modulator

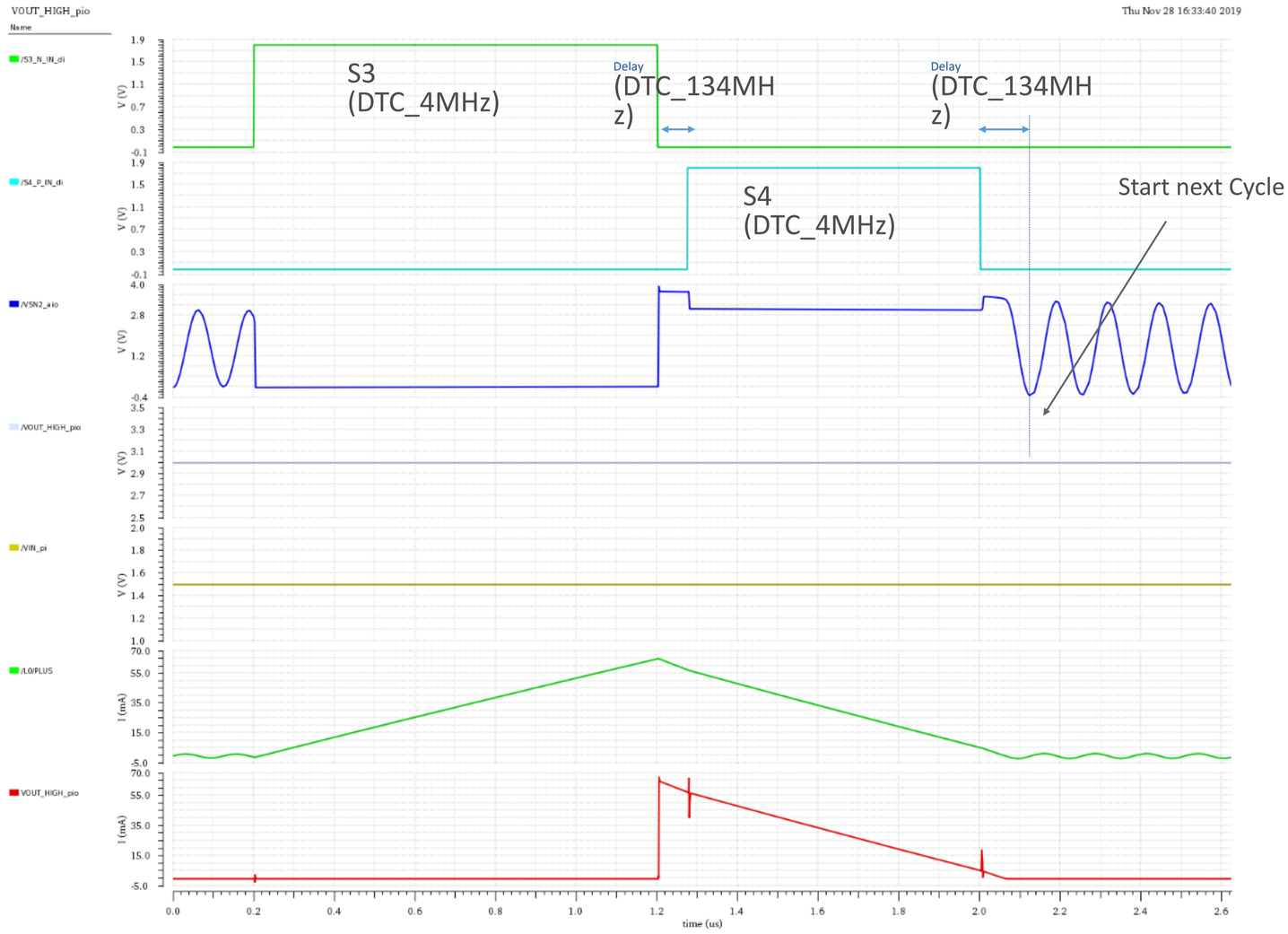
Waveforms for single cycle 3Vin, 22uH, 124mA_pk, ~300nJ transferred

Exaggerated intervals of S4 body diode conduction for illustration of SR

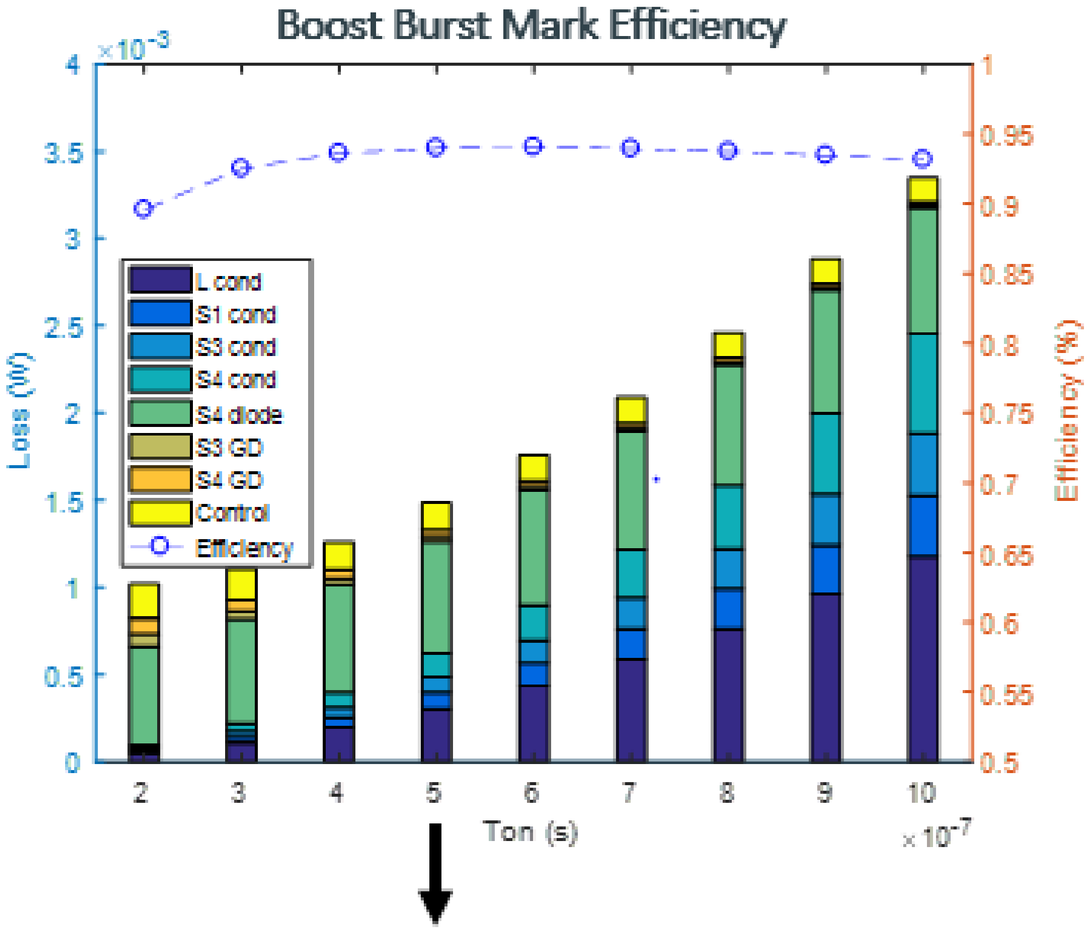
Note the low switch node damping

& Inductor DCR set high at 800mΩ for this simulation

Modulator waveforms by DSM building with DTC

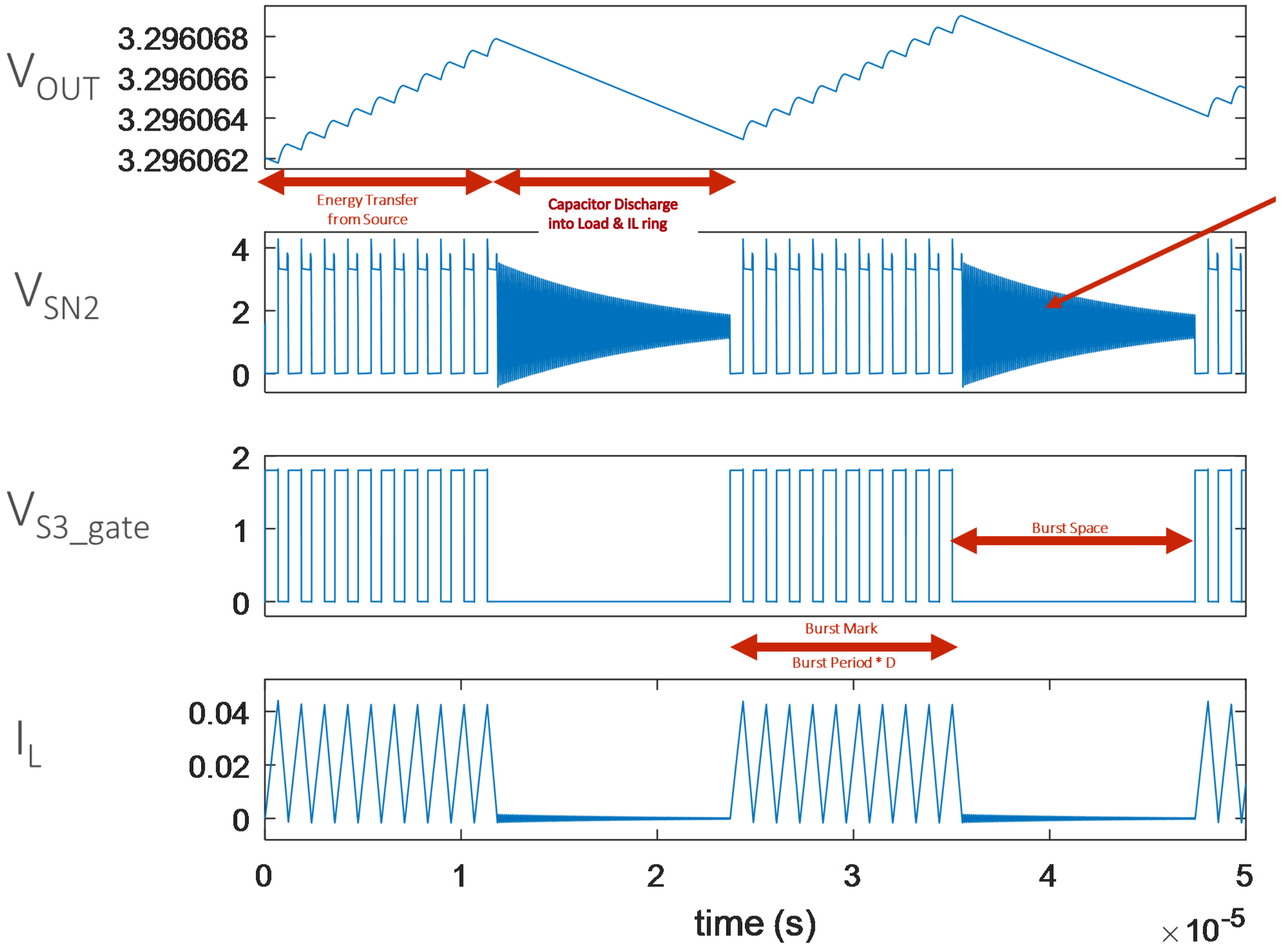


Optimised Per-Cycle Efficiency & Burst Mode



Vin=1.5V & V_{out}=3.3V

Max η @ t_{on}= 500ns, P_{mark}= 25.4mW



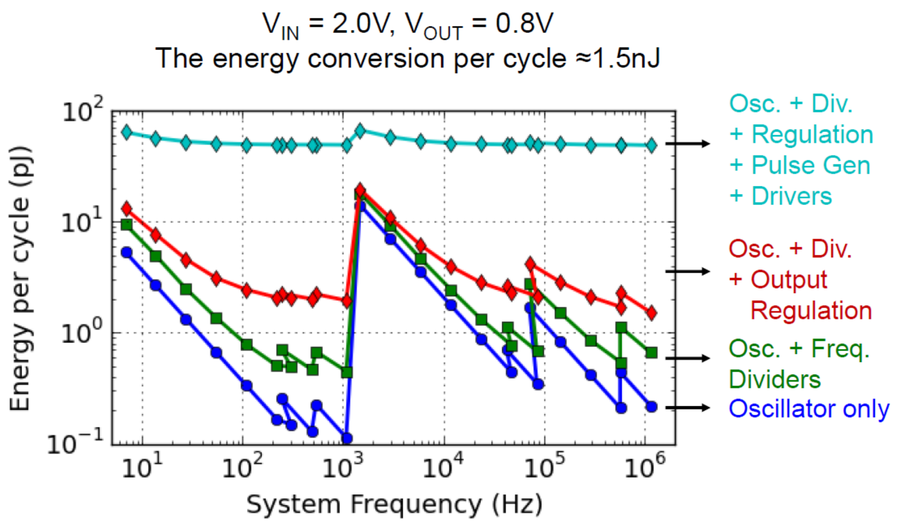
4-Switch Quasi-Resonant Buck-Boost Converter for Ultra Low Power in 180nm CMOS, **James McCarthy, Gerry McGlinchey, Madhu Jacob, Ivan O'Connell, Séamus O'Driscoll,** MTC - MCCI Technical Conference May 2019

Control & Drive Efficiency vs Research

(considering 100 X Po difference between these designs)

IBM, MIT Research ISSCC'17 65nm

Overall Control Energy Loss for 240 pW Quiescent (0.8mW *max*) Buck Converter 2V-0.8V, 47uH (65nm CMOS

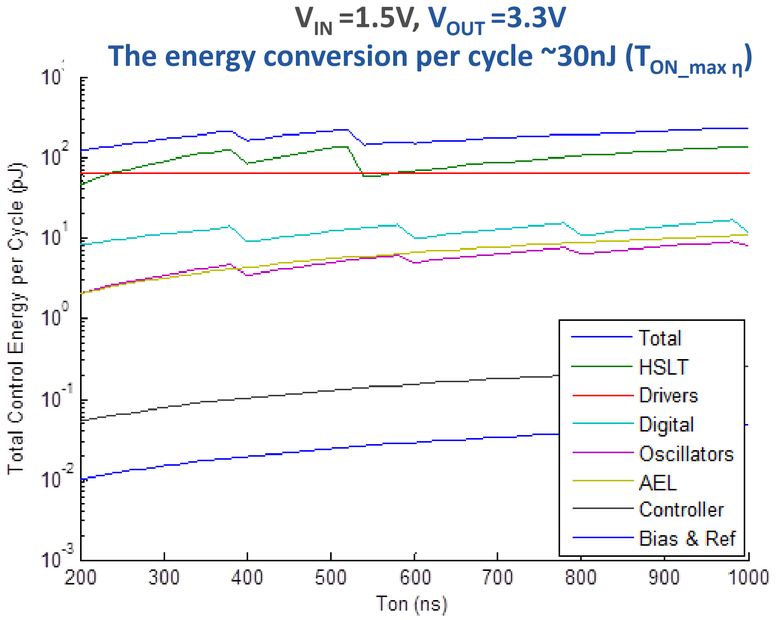


Energy Out ➧ (Control+Drive) Energy per Cycle => ($\eta_{CONTROL}$) = 95.6%

A Buck Converter with 240pW Quiescent Power, 92% Peak Efficiency and a 2x10⁶ Dynamic Range, Arun Paidimarri, Anantha P. Chandrakasan, ISSCC'17

Tyndall MCCI, Mischief 180nm (SCH SIM)

Overall Control Energy Loss for 200 nW Quiescent (27mW @$T_{ON\_max\ \eta}$) Buck-Boost Converter 1V5-3V3, 22uH (180nm CMOS)



Energy Out ➧ (Control+Drive) Energy per Cycle => ($\eta_{CONTROL}$) = 98.83%

(@ TON_max η = 600ns (max. η), S3_GD =27pJ, S4_GD=34pJ @ Ton = 600ns for 1V5 to 3V3, 1kHz/1ms Burst Space assumed = 200pJ

Timing Requirement: Nano-seconds to Hours

For the example: P_switching_cycle_optimised = 25.4 mW

=> Burst Space = 25.4 ms for 1uW Power, for one switching cycle (~ us) per burst

For a number of switching cycles per burst-mark; the burst space will be 100s milli-seconds

INTERLEAVED SOURCES may require vastly different switching cycle on-times and duty cycles, such as from HV Buck to LV Boost

Relatively large Energy per Switching Cycle is required for low Gating and Control loss

=> SMALL BURST DUTY CYCLES

ENERGY METROLOGY will require accurate timing during short on-pulse duration and during long off-time (hours, days)

Non-bursting control may be by LTI control and cater for high resolution count number. Low energy bursting may require small counter values => clock frequency flexibility

=> UNIFIED TIME BASE is required from 10s' ns to hours

Digital to Time Converters (DTC)

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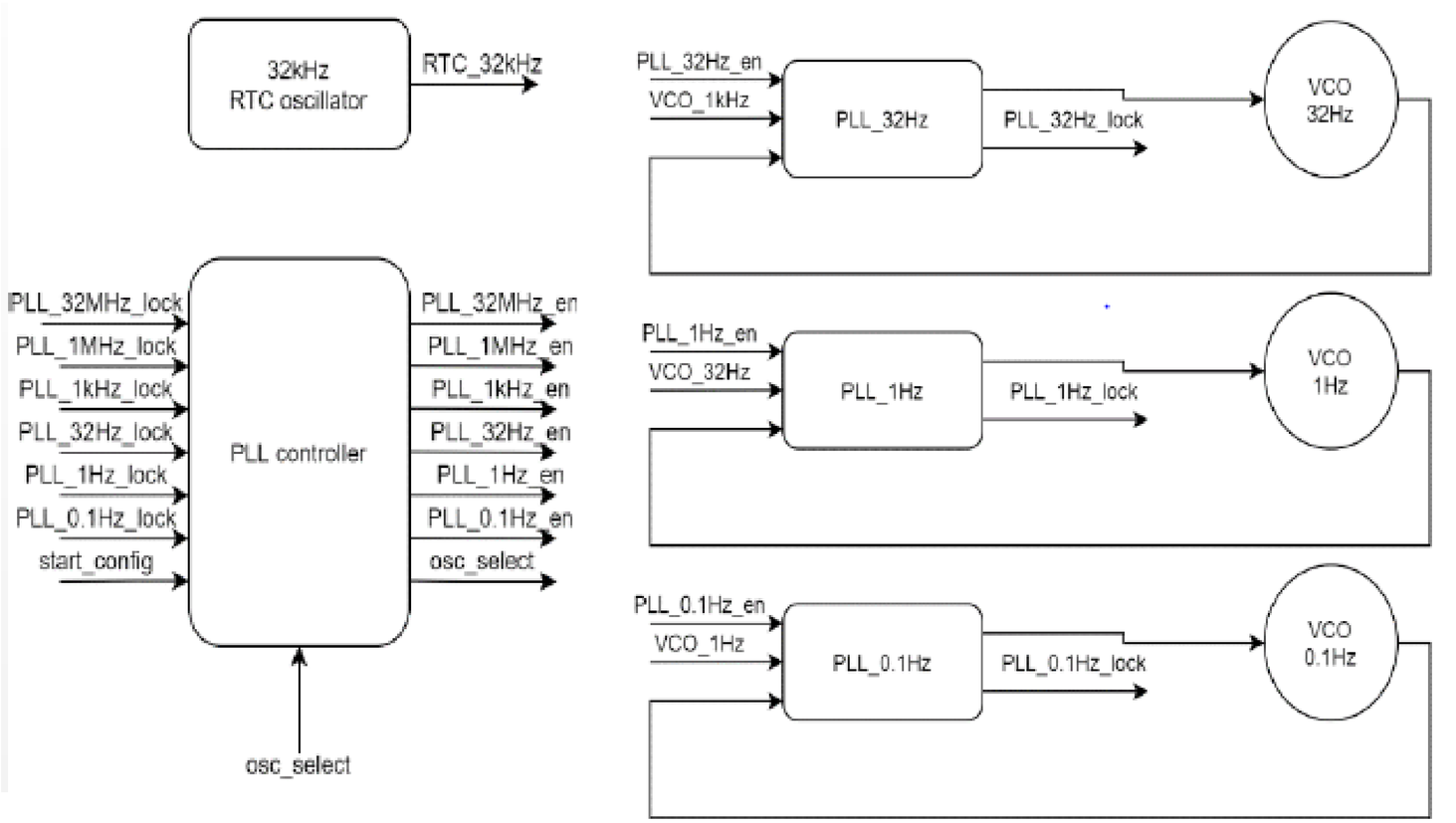
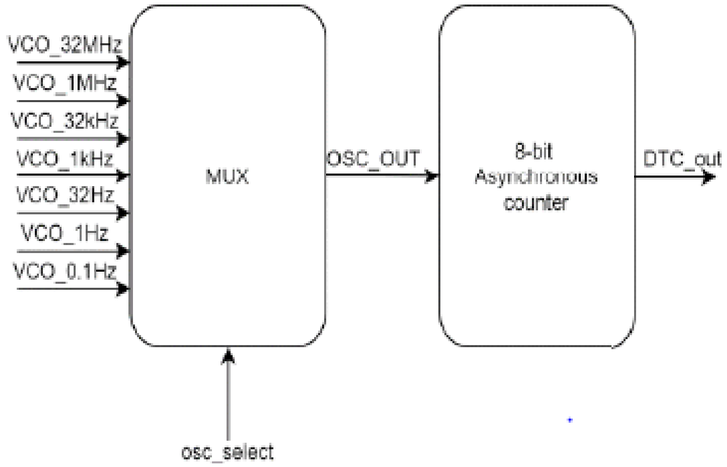
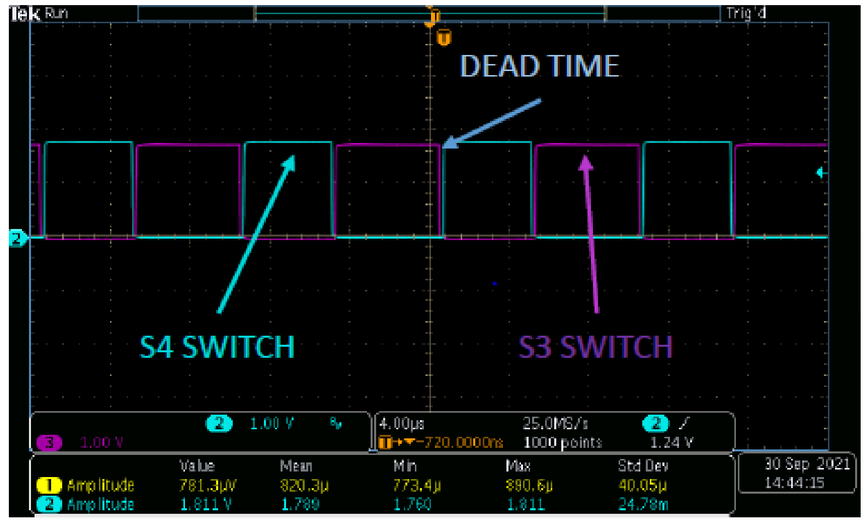
- Triggerable sequentially to build PWM or PFM Modulator Output
- Unified time base from 10 ns to hours
- Ganged system of 7 ultra low power oscillators, rapid start current-starved oscillators
  - 32 mHz to 32 MHz, and 134 MHz
- Background low energy PLL system to trim 7-Gang to the 32 kHz RTC
- 8b control over Ton
- 35b control over ***Toff*** or other ***Wake*** or ***Metrology Timing***
- Dynamic oscillator enabling and interchange for lowest energy interval counter during LTI control

DTC (PLL + LF OSC Bank + HF OSC Bank)







Energies (incl. oscillator start-up energy):

1 us - E = 244 pJ

1 ms - E = 92 pJ

10 ms - E = 306 pJ

1 s - E = 100 nJ

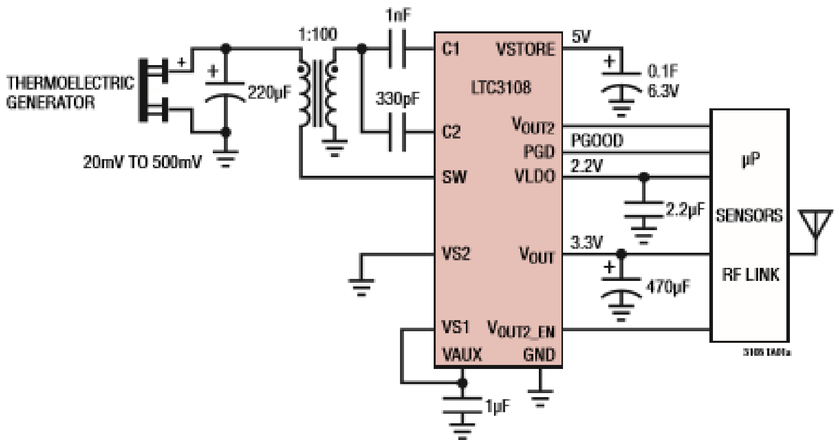
680 nW RTC

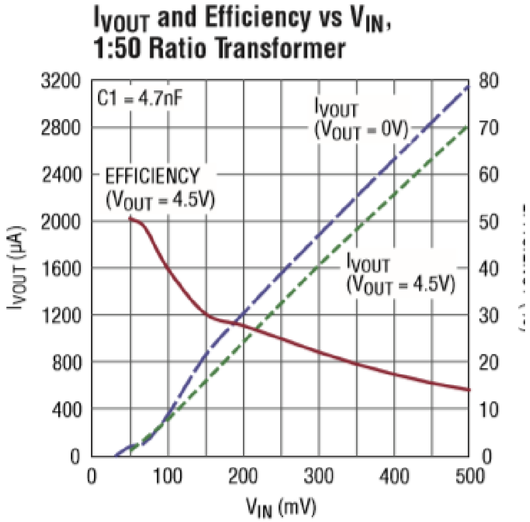
6 nW 0.1 Hz OSC

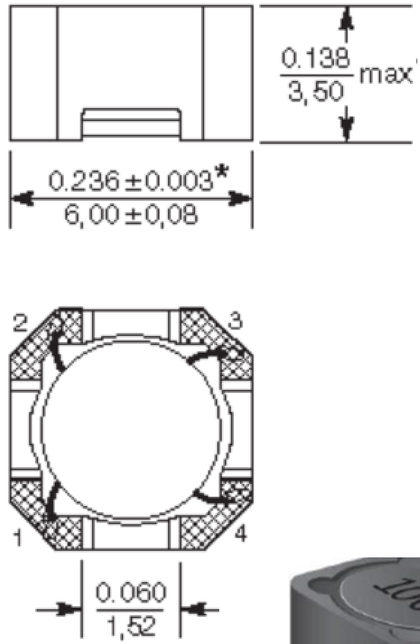
Measured Modulator Waveform with 4 DTCs in cascade, incl. 134 MHz Delay Counters

Commercial Low Voltage Cold Start

LTC3108







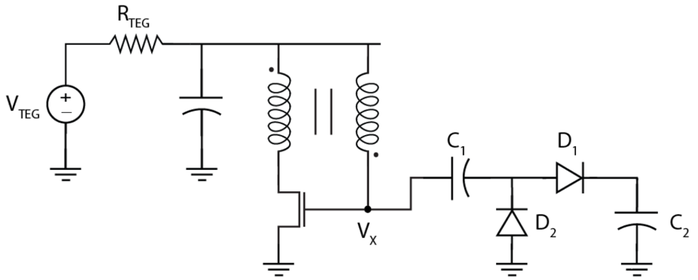
1:100 Tx => Start-up at 20mV, Iin > 3mA

f_0 recommended 10 – 100 kHz

Resonant 1:N coupled-inductor is relatively huge at **6 X 6 X 3.5** mm

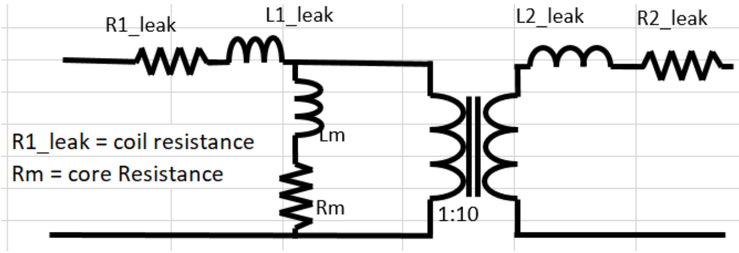
https://www.analog.com/media/en/technical-documentation/data-sheets/LTC3108.pdf

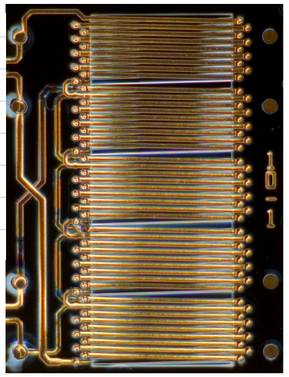
4:40 tf-MoS Meissner Oscillator based:



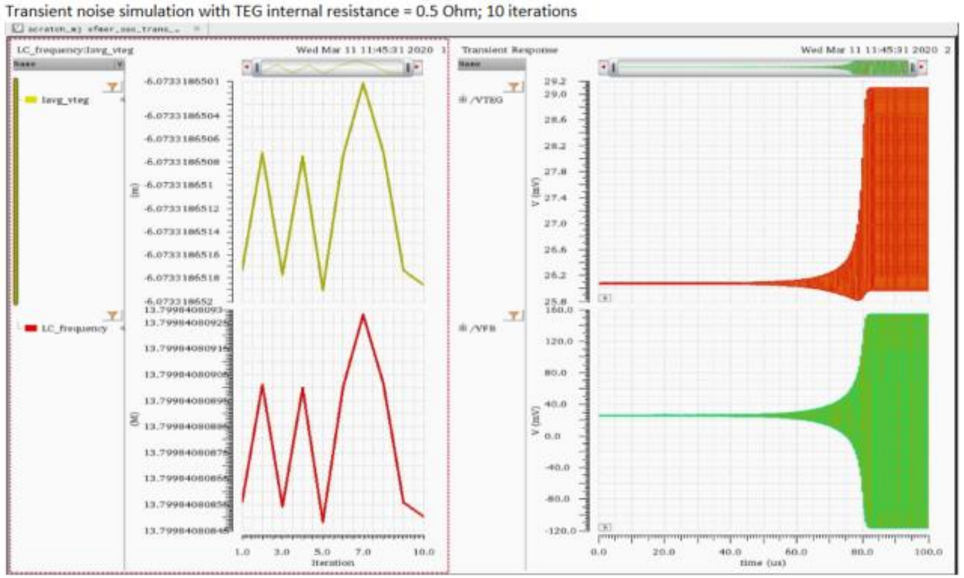
Meissner Oscillator [12]

	100 Hz	15 MHz	20 MHz
Lm [nH]	4	16.4	18.7
L1_leak [nH]	4	19.2	19.1
L2_leak [nH]	100	90	80
Rm [Ohm]	0.001	0.261	0.972
R1_leak [Ohm]	0.049	0.53	0.568
R2_leak [Ohm]	0.8	6.7	7.8





- 180 nm CMOS *simulation* using measured S Parameter Model:
  - 14 MHz = f_0
  - 4.2 mA Iin @ 30 mV (SCH)
  - 200 X 100 um Dep. Device
  - k ~ 0.65



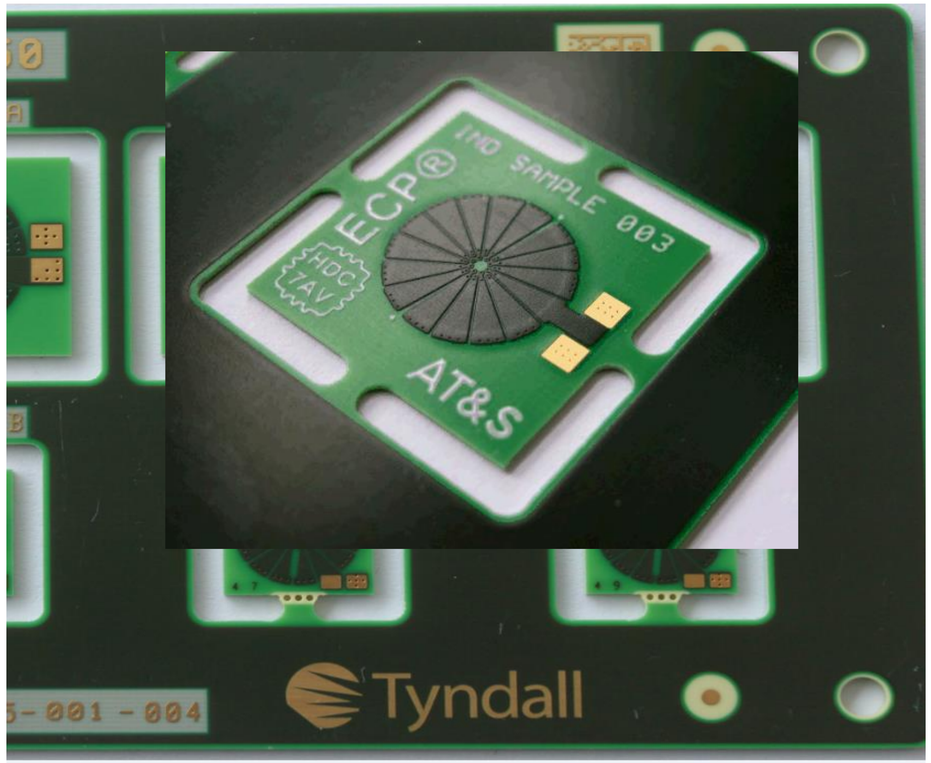
Feature	Dimension
Cu trace width	80 um
Cu trace thickness	16 um
Via diameter	100 um
Bond-pad diameter	160 um
Die size after dicing	4 × 5.2 mm^2
Die size before dicing	4.6 × 5.9 mm^2

"Ultra-low loss integrated magnetics platform for high frequency power delivery networks", Pranay Podder et al., Tyndall, Chor Shu Cheng et al., Global Foundries, 11th International Conference on Integrated Power Electronic Systems; Berlin, Germany. March24-26th, 2020

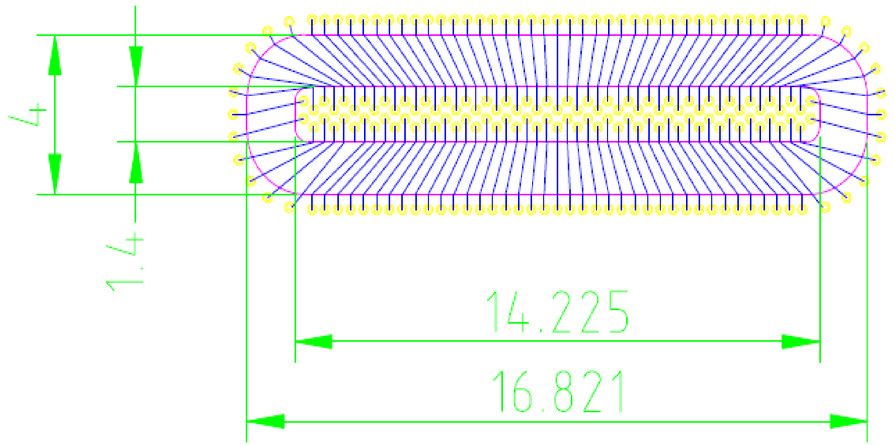
EU H2020 Grant No. 730957

IS505.7 PwrSoC: Industry Adoption in High Volume Applications, APEC 2022

Tyndall Cold –Start transformers



- ***PCB Embeddable Planar Toroidal*** Inductor
- Simulated – this version not fabricated
- 1:100 shown, 4 mm X 17 mm, (1:40 is half size)
- Commercial magnetic material
- I_{MAG} = 2mA, Iin = 6.6 mA, 7.5 MHz, Vin= 20mV (SCH SIM)



R. Murphy, Tyndall, et al., G. Weidinger et al., AT&S, EU H2020 "GaNonCMOS" www.ganoncmos.eu, CIPS2020
"High Frequency Magnetic Sheet Materials – Performance Factor Comparisons and Design of
Toroidal Inductors Embedded in PCB", Ruaidhrí Murphy et al. APEC 2021

COLD-START:

Get the system going from low, unregulated voltage

	MoS Transformer based Oscillator	ECP transformer based oscillator	LC tank based Oscillator	Ring Oscillator
On-chip area	2mm x 1mm 6mm x 4.5mm	2mm x 1mm	2mm x 1mm	3mm x 1mm
Off-chip area	None	16mm x 4mm (PCB embedded)	16mm x 4mm (PCB embedded)	None
Vstart-up	80 mV	40 mV	150 mV	175 mV
Power required for start-up	480 uW	240 uW	15 uW	5.3 uW

Status:

On-chip 380 mV block taped out in H1M2

3 blocks at Schematic PVT to tape-out H2M3 Q1 2022

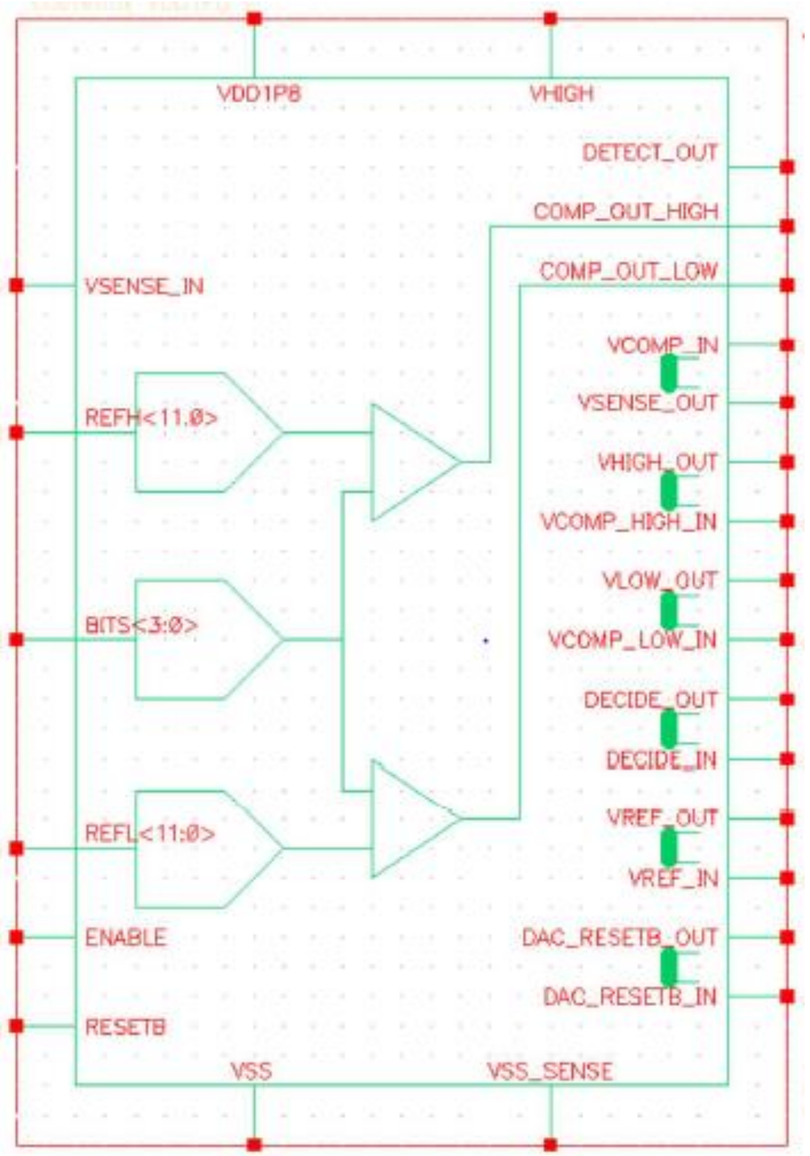
JRA CC 01/06/2021

DYNAMIC BANDGAP REFERENCE

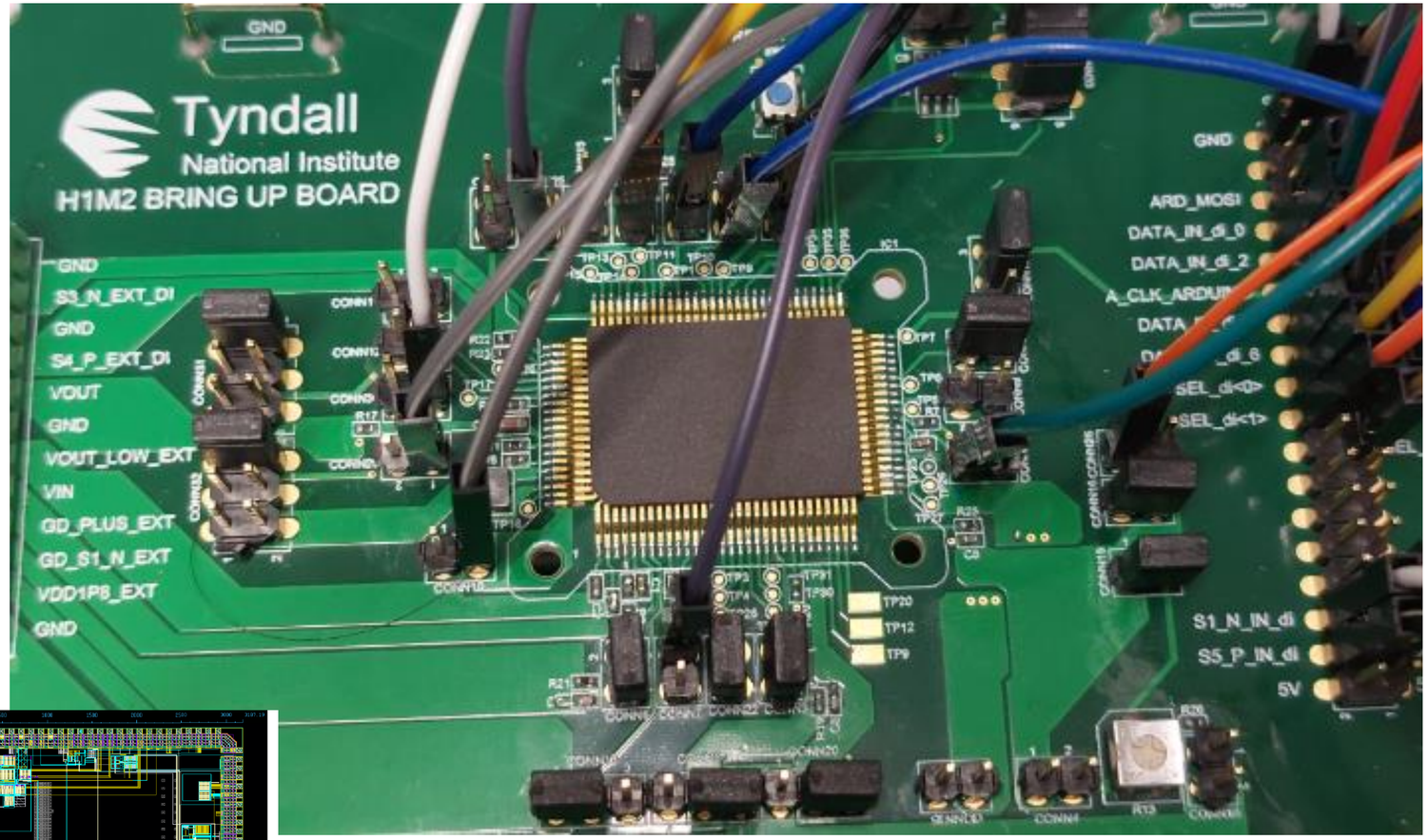
Powers Up, Settles and drives
Dynamic Hysteretic Voltage Sense

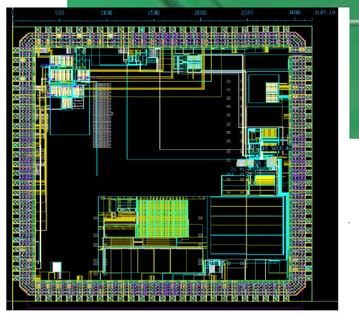
Or ***12 bit Precision Differential SAR ADC***

~ 15 uA for 15 us = 225 pJ



Ultra Low Power “Mischief” PMIC PLATFORM for Energy Harvesting IoT Node



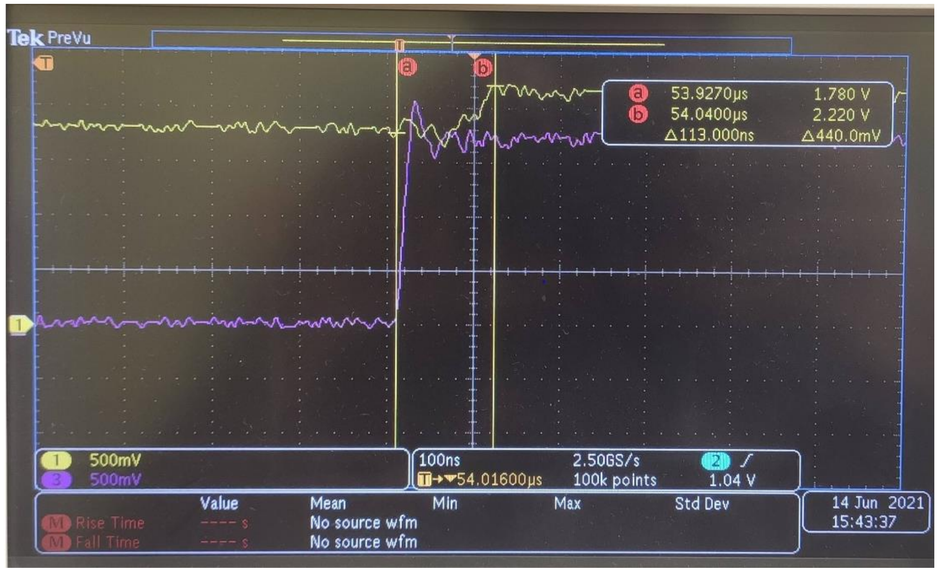


H1M2 v1 IC – Most blocks are working as intended.

RING_VDD_1P8 = 18 nA
GD_VDD_1P8 = 20 nA

Preliminary H1M2 chip tests

VHI Block: Selects the highest voltage in the system VIN, VOUT, VBIAS, V_PRI_BAT, V_STORAGE must always be available to bias the bodies of PMOS devices by a clocked-comparator multiplexer system



Output voltage changes when VIN2 transitions to 2 V, while VIN1 is at 1V8

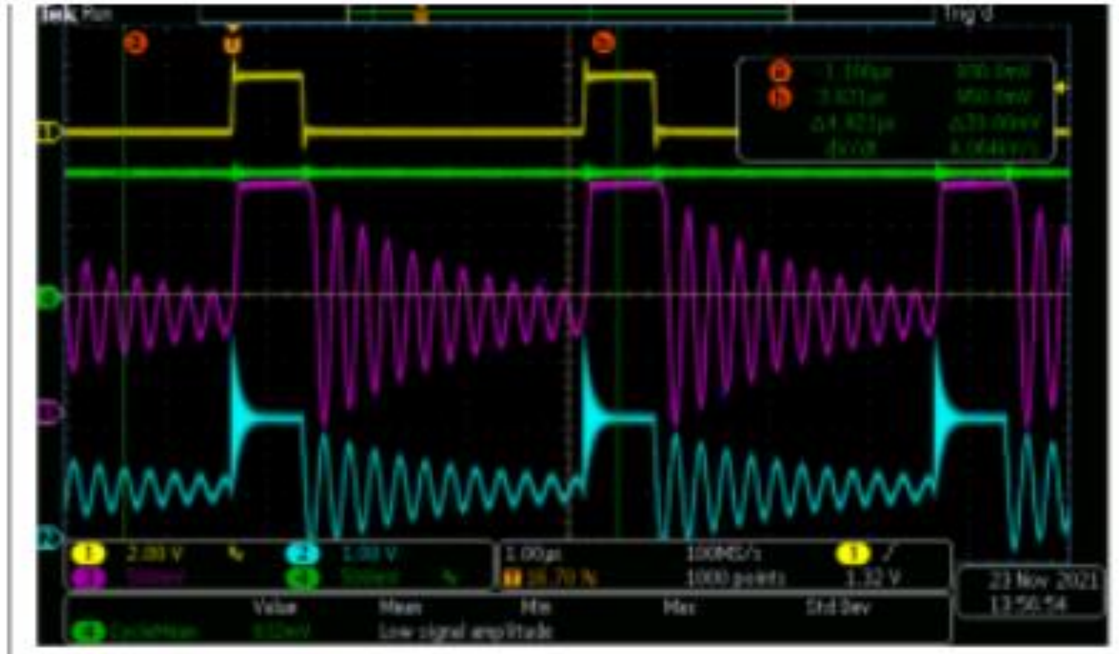
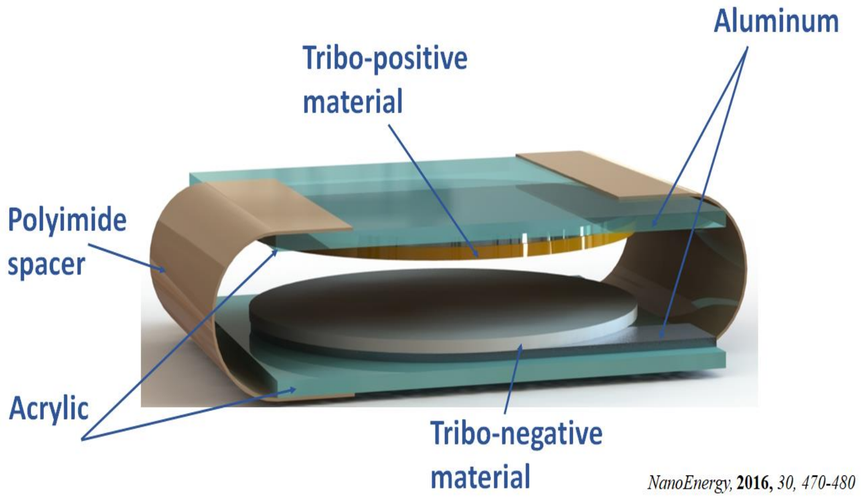


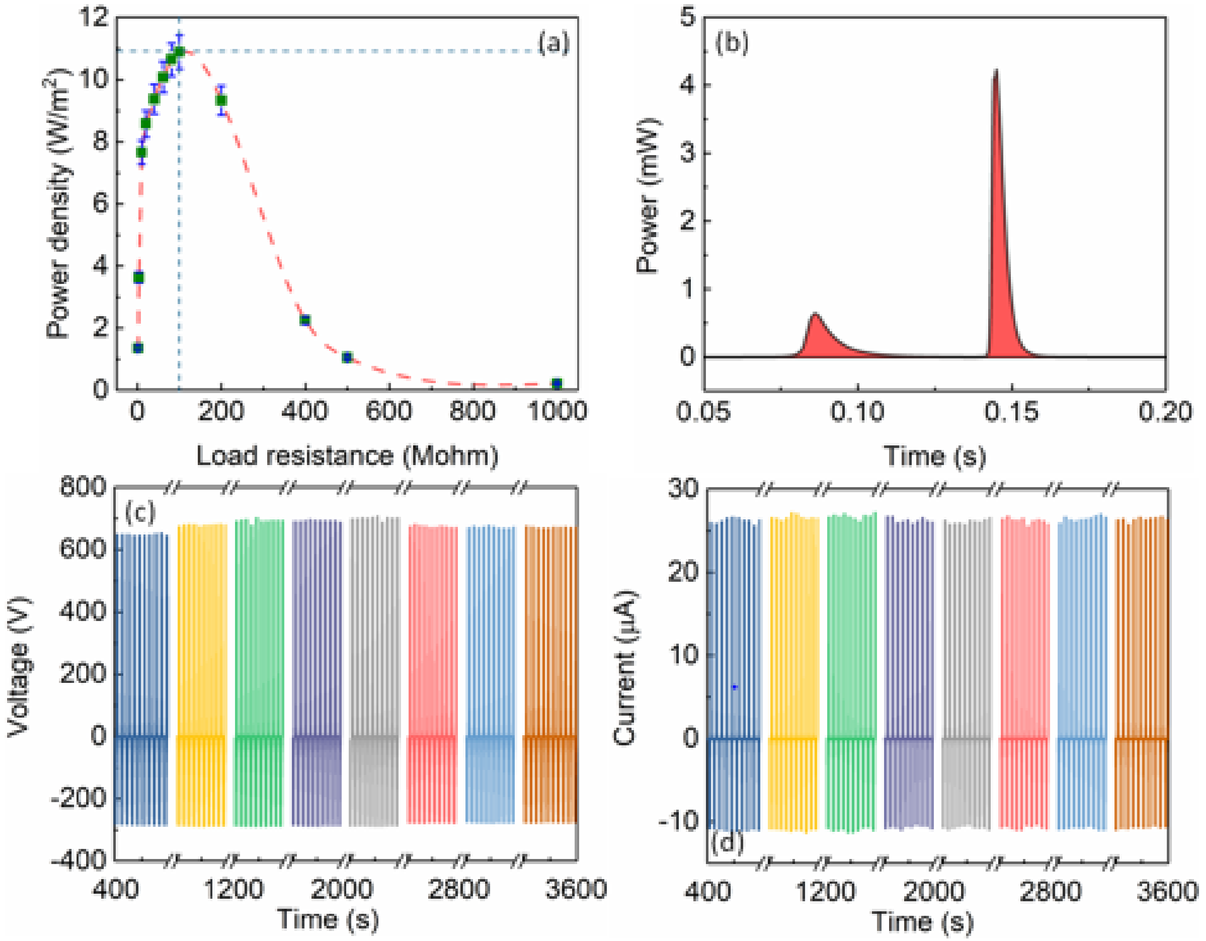
Figure 21: Power path switching cycles for Vin = 1.8 V (modulating signal – yellow, Output voltage – green, VSN1 – cyan, VSN2 - magenta)

Tribo-electric Generator - TENG

EnABLES TA 051 Dr Navneet Soin, Ulster University



NanoEnergy, **2016**, *30*, 470-480



https://pubs.rsc.org/en/content/articlelanding/fd/2014/c4fd00159a#!divAbstract

https://www.sciencedirect.com/science/article/pii/S221128551930998X

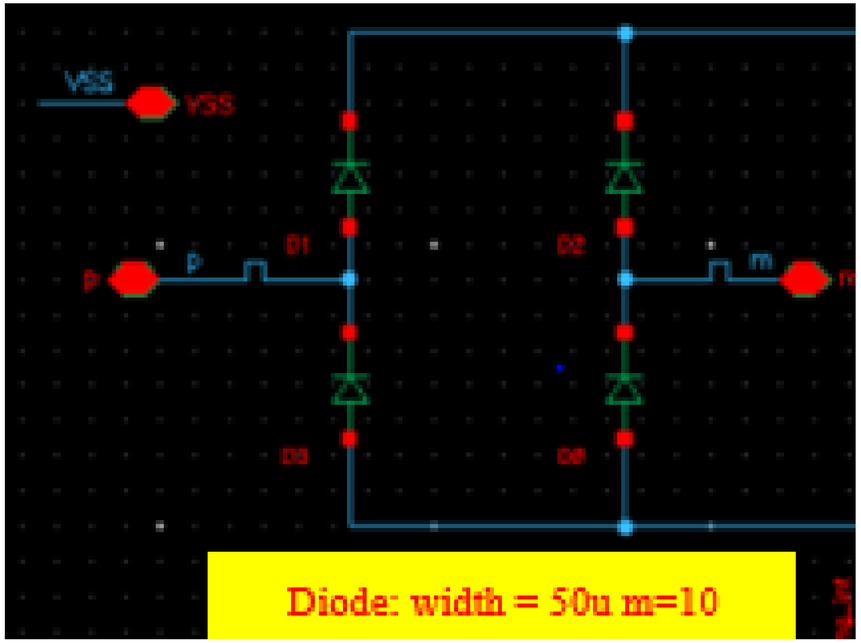
https://www.sciencedirect.com/science/article/abs/pii/S2211285518300430

https://pubs.acs.org/doi/abs/10.1021/acsami.7b18442

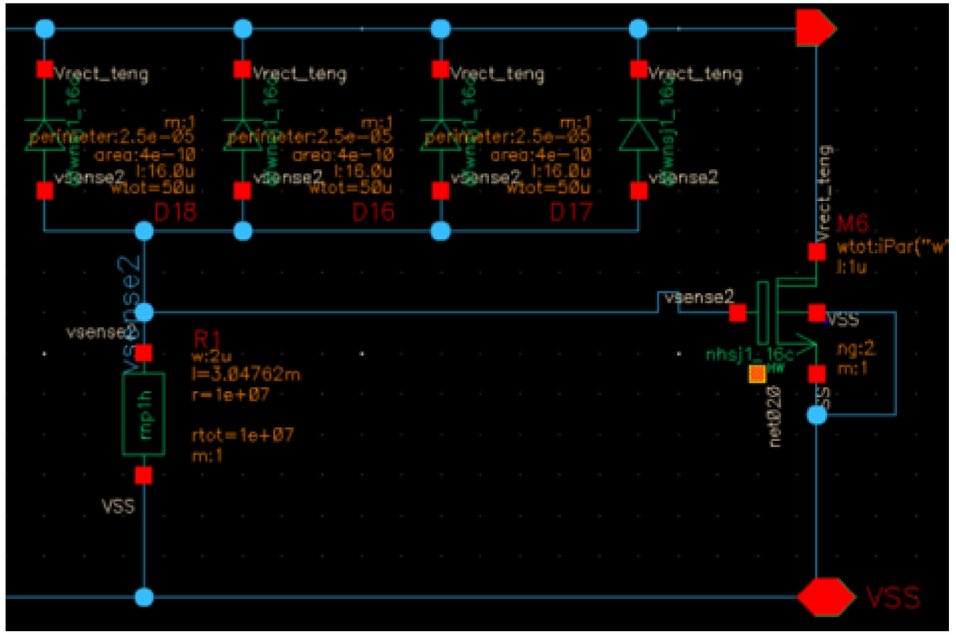
https://www.sciencedirect.com/science/article/abs/pii/S221128551630458X

CLAMPED 200 V DIODE BRIDGE + 200 V Buck Converter

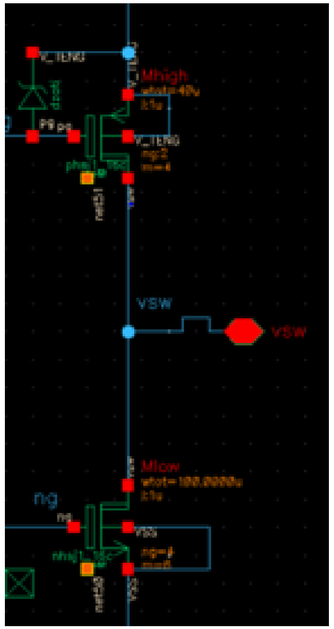
Using XFAB 180 SOI: 200 V SJ FETs and Diodes & Clamping to 200 V



200 V Bridge Rectifier



200 V Clamp



200 V, 30 kHz Buck Converter 4 mW 80 % efficient

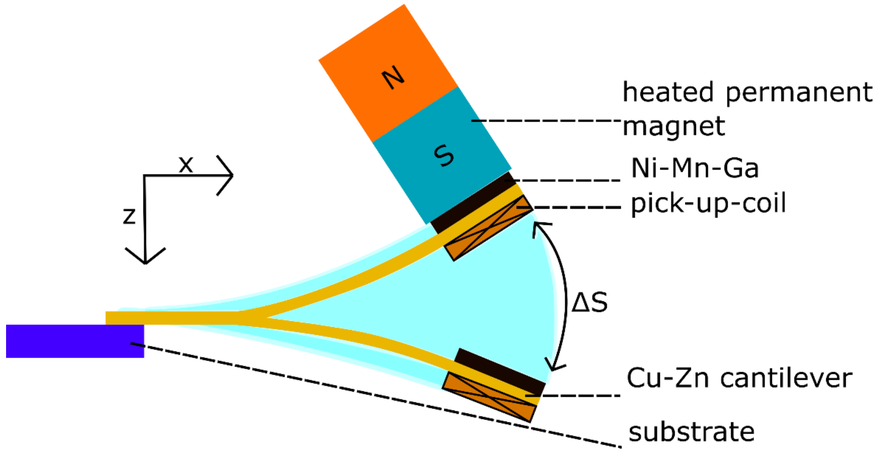
TMG: Thermomagnetic Resonator

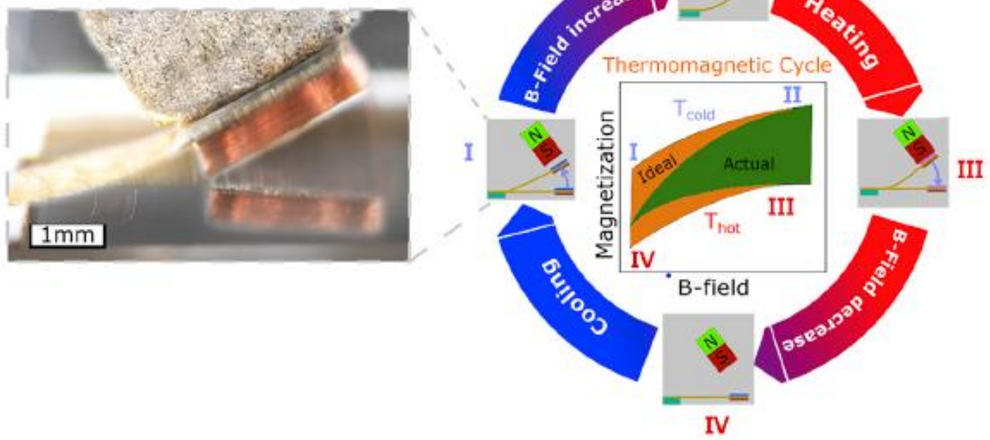
Enables TNA_052 Feasibility Study: Tyndall + Manfred Kohl, KIT

Karlsruhe Institute of Technology

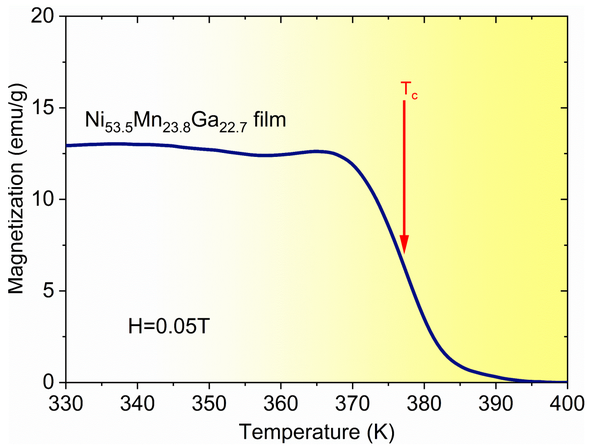
Institut für Mikrostrukturtechnik
Institute of Microstructure Technology

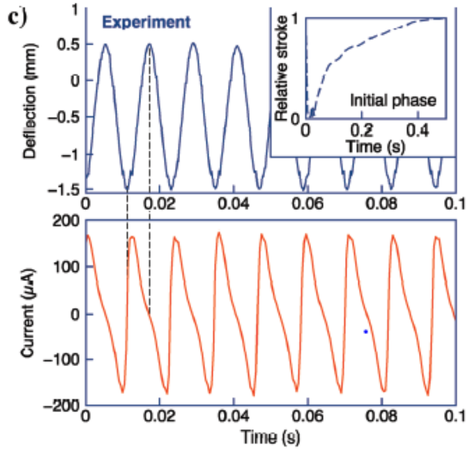
Tyndall National Institute
Institiúid Náisiúnta





Heusler alloy films



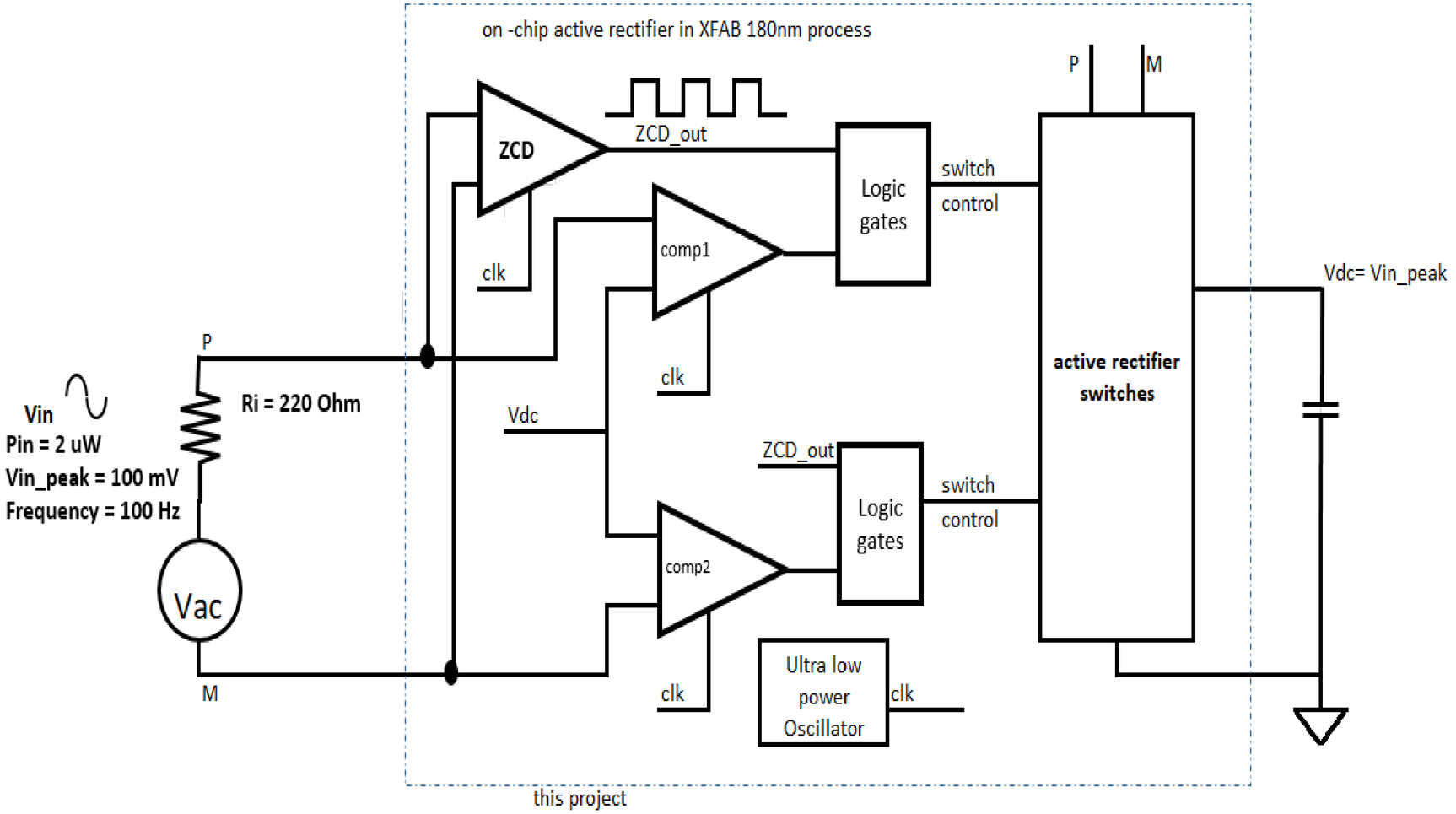


- Designing an Active Rectifier block to interface this AC voltage source with *Mischief*
- Efficiently convert 10-100 mV AC, ~100 Hz, 2-5 µW

J. Joseph, et al., *Upscaling of Thermomagnetic Generators Based on Heusler Alloy Films*, Joule 4,12 (2020) 2718-2732.
DOI:10.1016/j.joule.2020.10.019

EnABLES EU H2020 Grant No. 730957

30 mV to 1 VAC Active Rectifier – 5uW +



100 Hz AC

10 kHz Clocked Comparator System

SCH level block design

SECE Piezo Harvesting Circuit Example

EUROSENSORS 2014, the XXVIII edition of the conference series

Quasi-Synchronous Charge Extraction for Improved Energy Harvesting from Highly Coupled Piezoelectric Transducers

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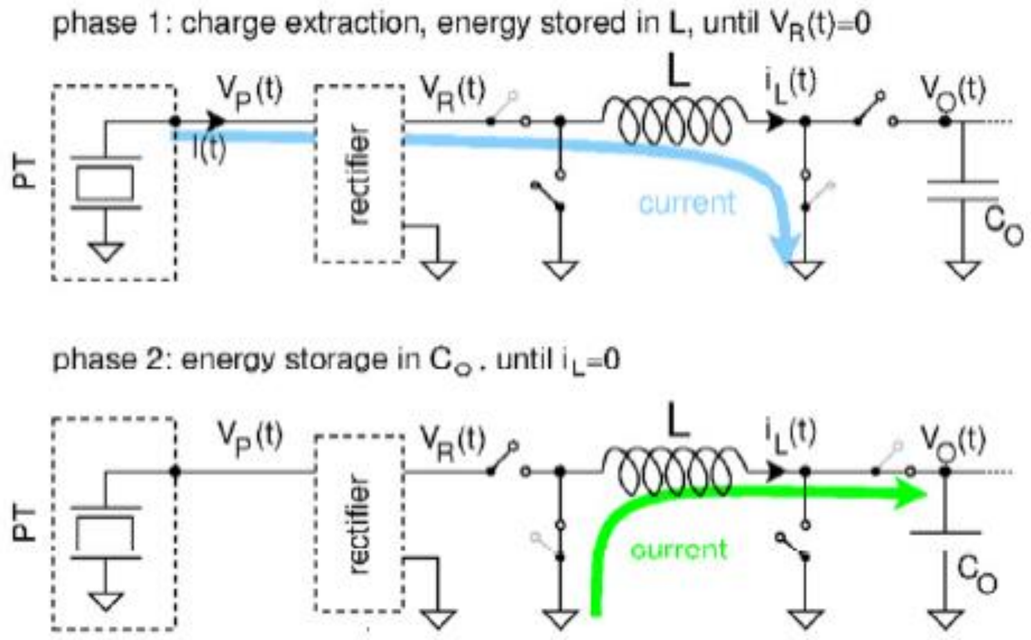

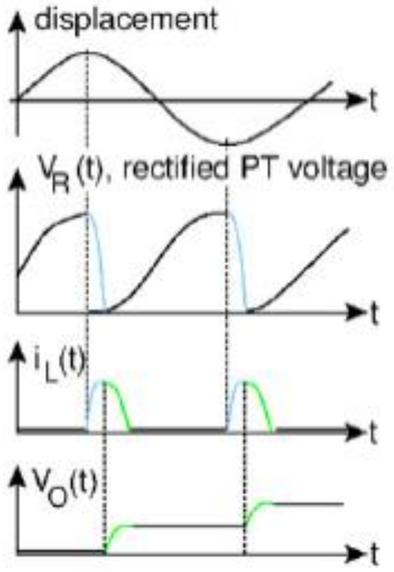

This is a Buck-Boost Circuit operated synchronously with mechanical vibration to resonantly (efficiently) extract charge from the piezo capacitive source

All of these harvesting circuits benefit from:

- MPPT
- Analog Event Driven State Machines
- Digital Timing Curcuits
- High Speed Low Threshold Comparators

EnerHarv 2018

Mechanical and Electrical Co-Design VEH

- **Mechanical Non-Linearities** added in transducer design +
- **Non-Linear Electrical Stimuli** to maintain high energy branch resonances
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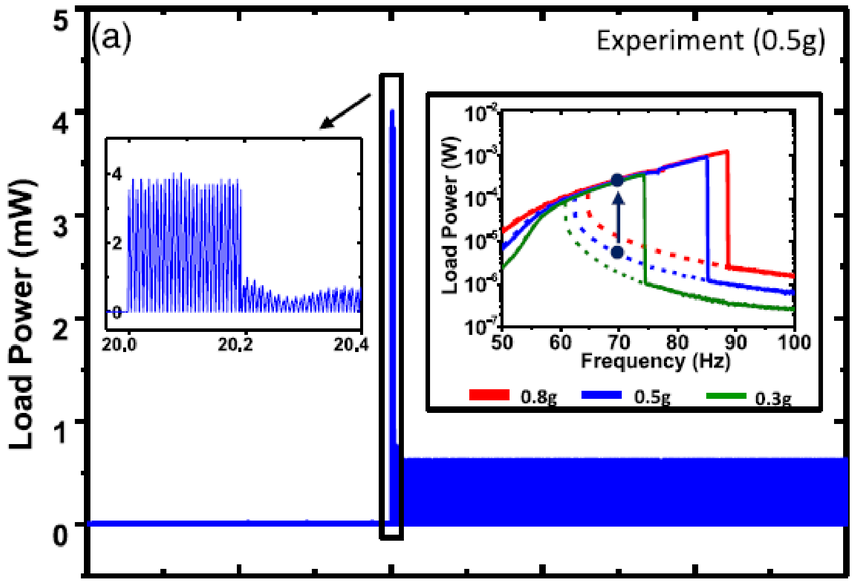
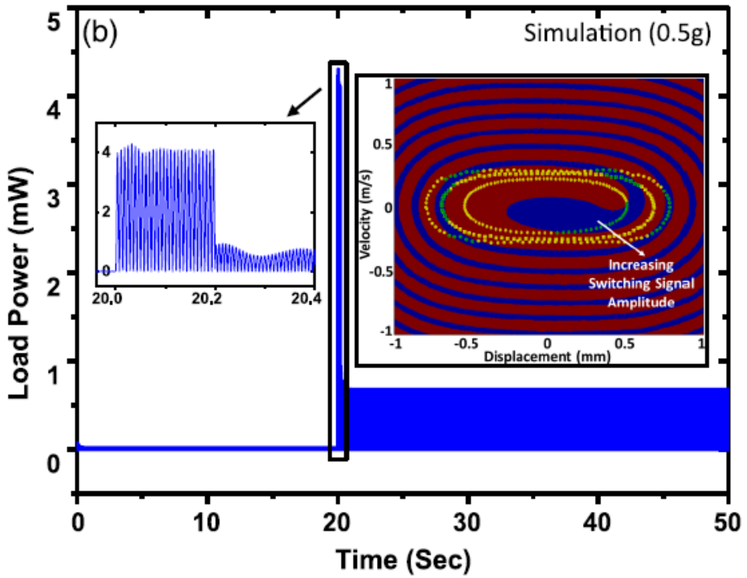
“‘Surfing the high energy branch of nonlinear energy harvesters’, D. Mallick, S. Roy, Phys. Rev. Lett., week ending 4 NOVEMBER 2016, claim

Example for Electromagnetic VEH





Conclusions

Currently we are engineering towards H2M3 version with 2nd revision blocks, plus new DTC/Modulator and ADC System

- All of the tough Analog blocks are then completed

Next stage is to seek ambitious system co-developer/ customers for a commercial prototype grade version

- Top Level Application Manager (Digital Block Design)
- Engineering to commercial grade platform, BIST

We welcome research collaborations and we are able to set up leveraged funding opportunities with Irish Government, EU or possibly US/Ireland Funding

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BACKGROUND IP
PMIC Technology Blocks

FLEXIBLE POWER PATH
OSCILLATORS & DTC
MODULATORS
BANDGAP & REFERENCES
COLD START
ADC
HYSTERETIC CONTROL
COMPARATORS
DC/ AC INPUTS/ RECTIFIERS
SPI - Digital Interface
DTI CONTROL
50 mV to 1 VAC Active Rectifier
5 - 200 VAC Rectifier & Buck Converter Front End

+

FOREGROUND IP
(IMT) Application ASIC

(IMT) APPLICATION MANAGER BLOCK (Digital)

(IMT) TOP LEVEL DESIGN - Interrconnecting Blocks

(IMT) APPLICATION BIST

APPLICATION QUALIFICATION

FABLESS SUPPLY CHAIN