EnerHarv 2024

PSMA International Workshop | 26-28 June, 2024 | Perugia, Italy

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EnerHarv 2024 Workshop:

DC-DC Switched Capacitor Converters: Design and Novel Solutions for the Energy Harvesting

Presented By –

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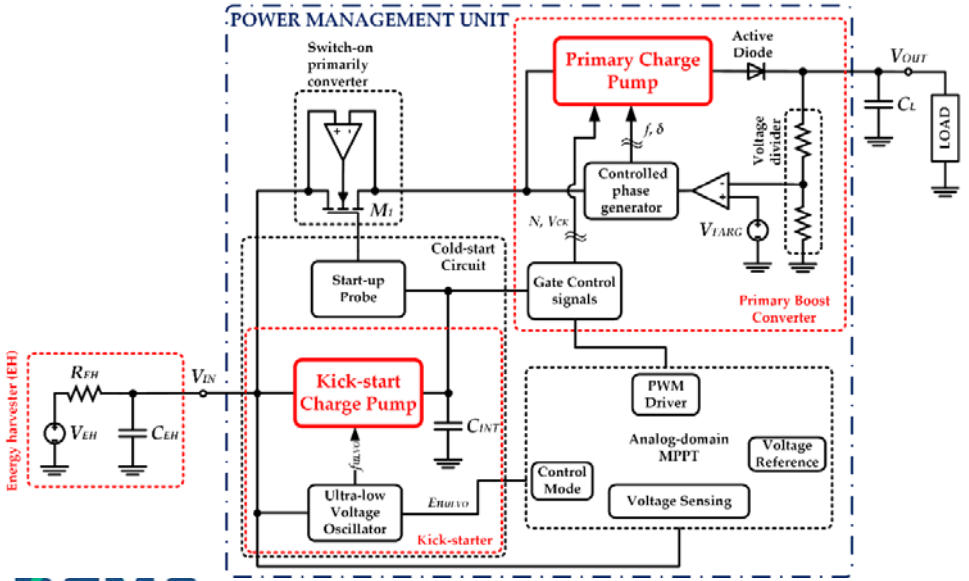
OVERVIEW

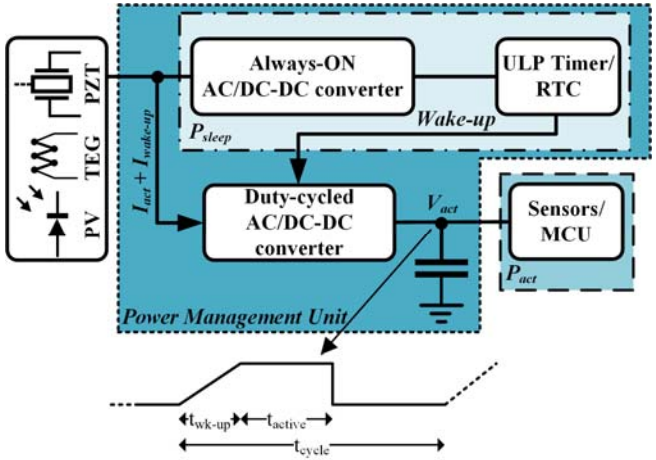
- **The charge pump: a ubiquitous block in modern applications**
- **The specific case of CP for single PV-cell: conventional schemes and the proposed one**
- **The specific case of CP for TEGs: drawbacks and a solution to alleviate them**

Charge pump: an ubiquitous block in modern applications

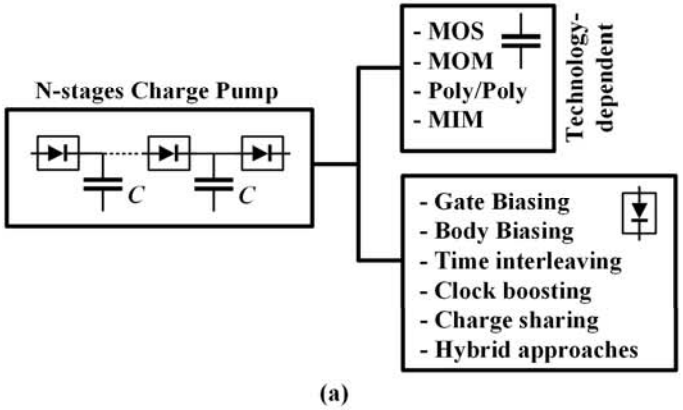
Applications such as self-powered ICs and energy-autonomous nodes work in duty-cycled mode and require **high efficient Power Management Unit** to gather the highest possible energy.

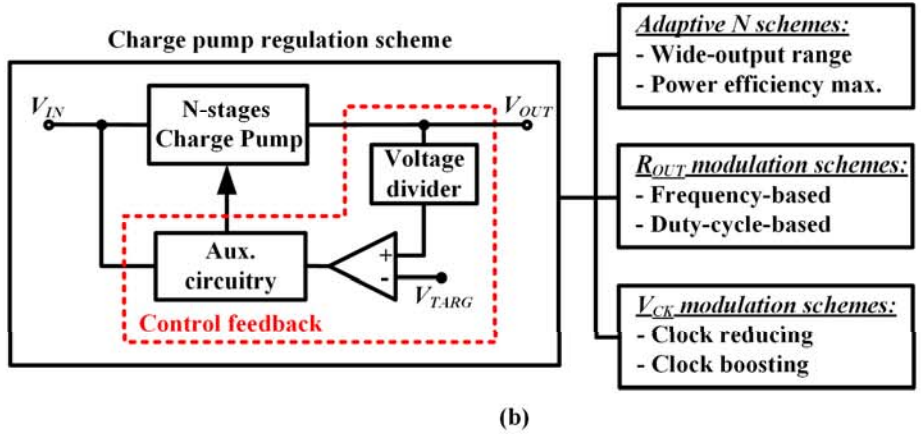
In these, a reduction of the minimum input voltage for the wakeup and the operations of the converter allow to work also with stringent conditions, improving the whole chip performances.

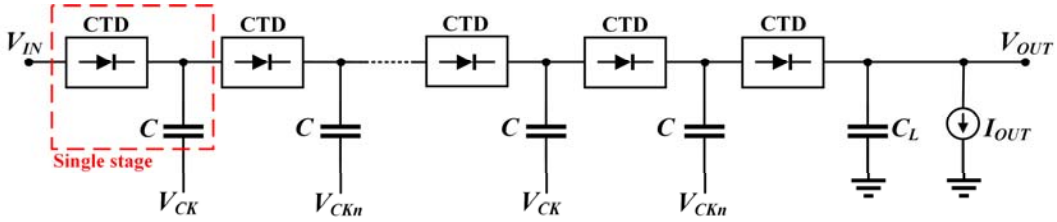




Conventional output voltage regulation schemes



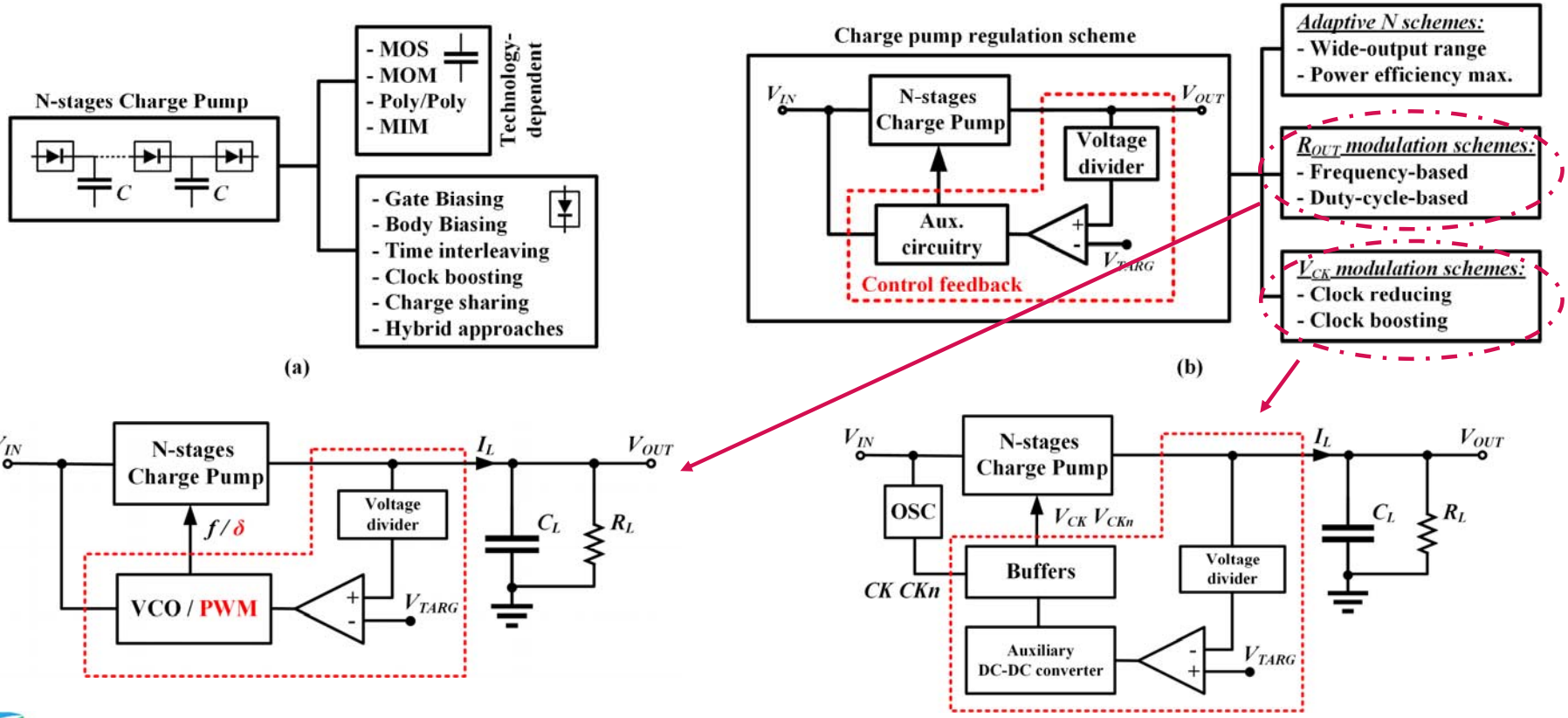




$$V_{OUT} = V_{IN} + NV_{CK} - R_{OUT}\, I_{OUT}$$

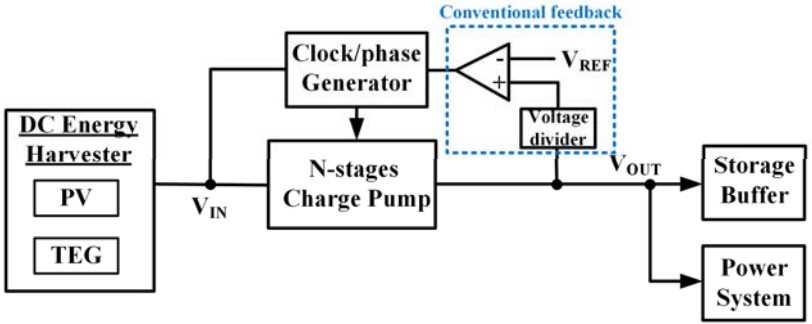
$$R_{OUT} = \begin{cases} {}^{N}/_{fC} & for\ SSL \\ (N+1)\,{}^{R_{CTD}}/_{\delta} & for\ FSL \end{cases}$$

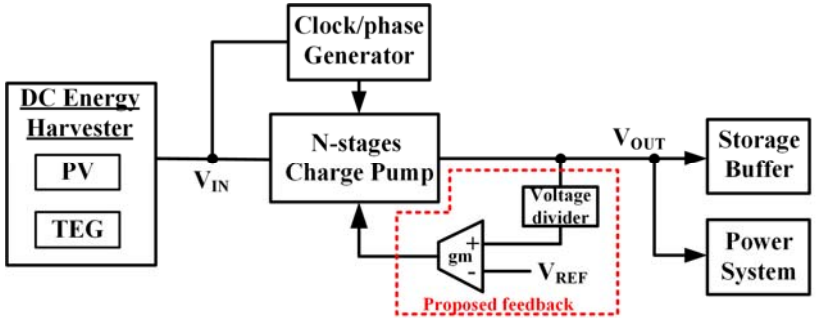
Conventional output voltage regulation schemes



Conventional output voltage regulation scheme vs. proposed one

- **We introduce a novel current-based regulation (parallel regulator) that exploits the bulk terminal of PMOS devices of the CP without entailing the clock/phase generator (conventional scheme).**
- **This strategy allows the reduction of the circuit complexity and of the minimum supply voltage while maintaining high power conversion efficiency.**





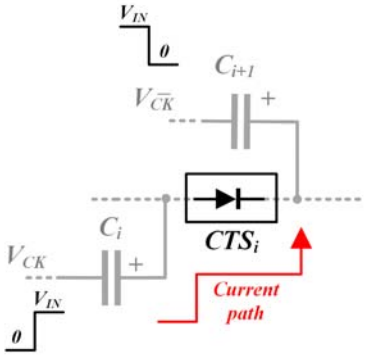
The proposed scheme

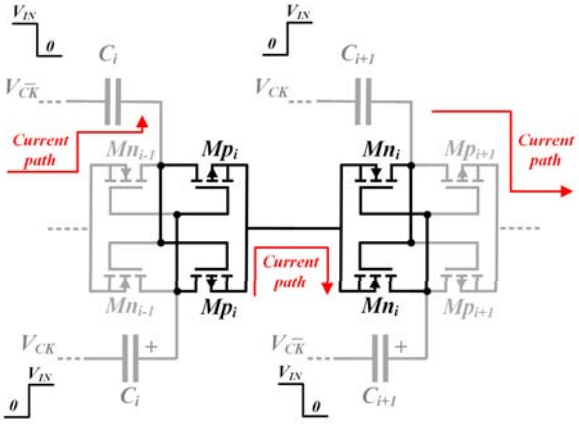
PROS:

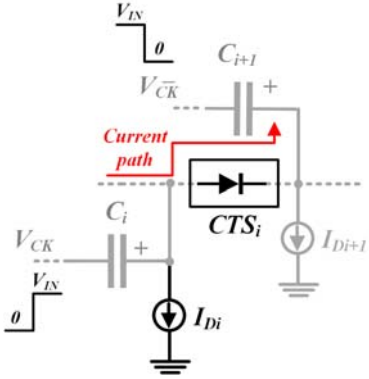
- **Allows the reduction of the circuit complexity and of the minimum supply voltage while maintaining high power conversion efficiency**
- **Low area overhead**

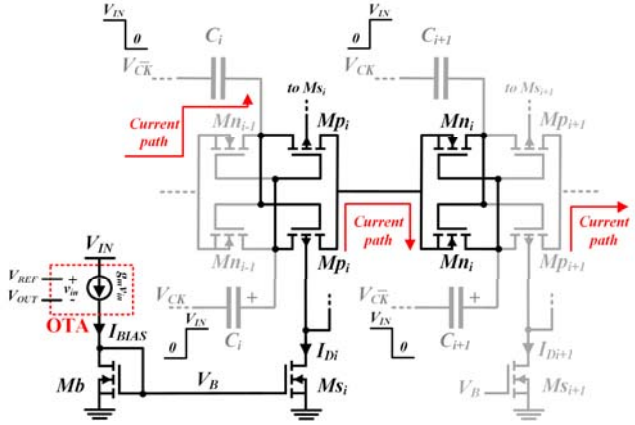
CONS (POSSIBLE):

- **Triple-well technology is suggested**









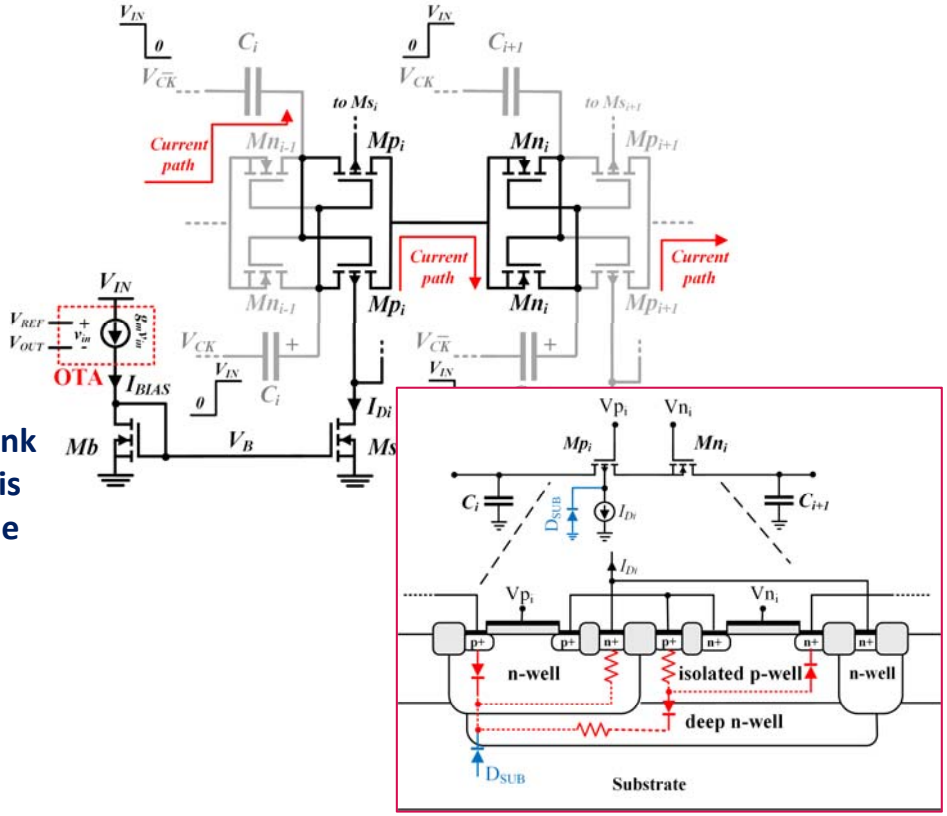
Remarks on transistor level implementation

The triad PMOS-source/nwell/ substrate shapes parasitic junctions that, inevitably, are turned on.

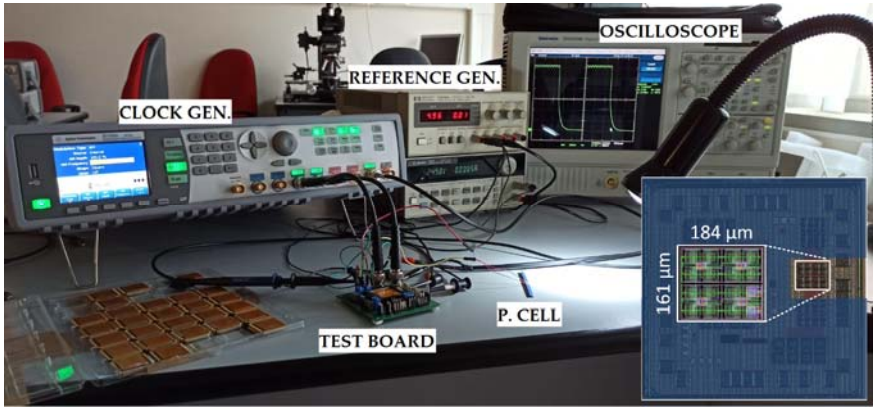
This aspect, which is detrimental for many applications, is instead a strong advantage for the proposed solution.

If the parasitic transistor is turned on, the actual current sunk from the capacitor is amplified by a factor (β + 1), where β is the common-emitter current gain of the transistor. From the point of view of the regulation loop, such amplifying factor contributes to increase the loop gain and, therefore, the accuracy of the regulated output voltage.

$$A_{cl} = 1 + \frac{(N+1)V_{IN} - I_L R_{OUT,CP}}{g_m(\beta+1)[(N+1)R_{CTS} + R_{OUT,CP}]V_{Targ}} \approx 1$$

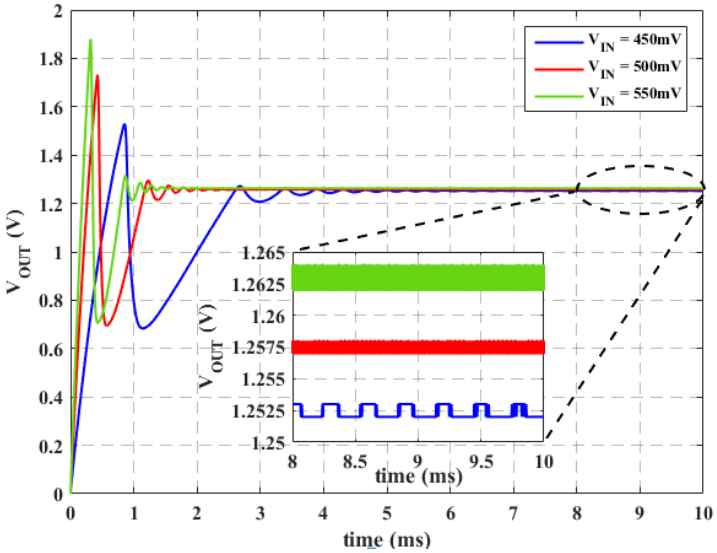


Simulation and measurement results



Measurement setup and layout of the charge pump superimposed to the chip micro-photograph

Simulated transient behaviour with only capacitive load



Line Regulation = ±107 µV/mV

Simulation and measurement results

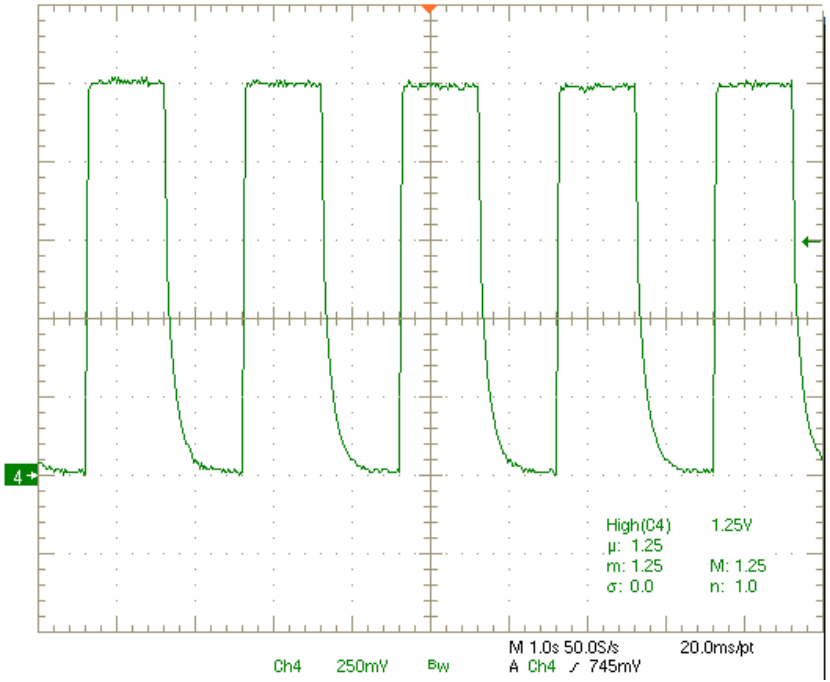
COMPARISON BETWEEN THE REGULATION SCHEMES

	Scheme	Working zone	Complexity
I_D	Current	SSL/FSL	low
N	Adaptive	SSL	high
R_{OUT}	Frequency/Duty-cycle	SSL/FSL	medium/high
V_{CK}	Reducing/Boosting	SSL/FSL	high

$$V_{OUT,SSL} = (N+1)(V_{IN} - R_{CTS} I_D) - \frac{N(I_D + I_L)}{fC}$$

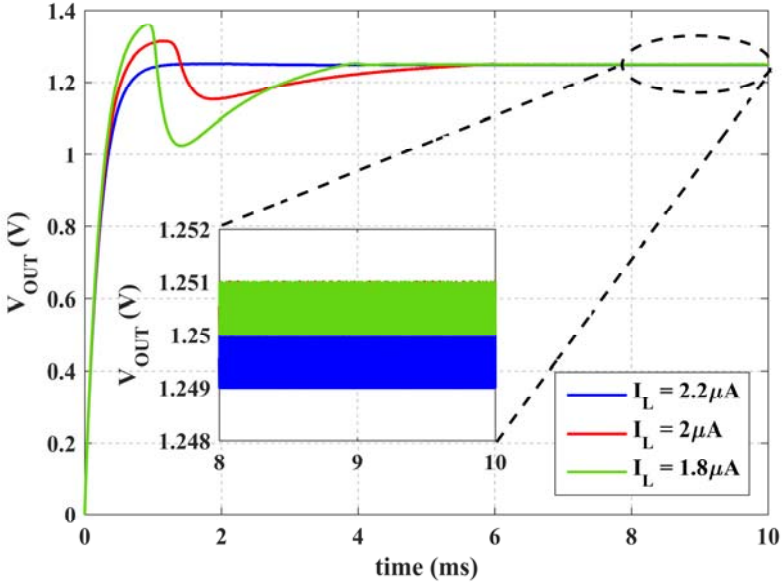
$$V_{OUT,FSL} = (N+1)[V_{IN} - R_{CTS}(2I_D + I_L)]$$

Output voltage: measured steady-state behaviour

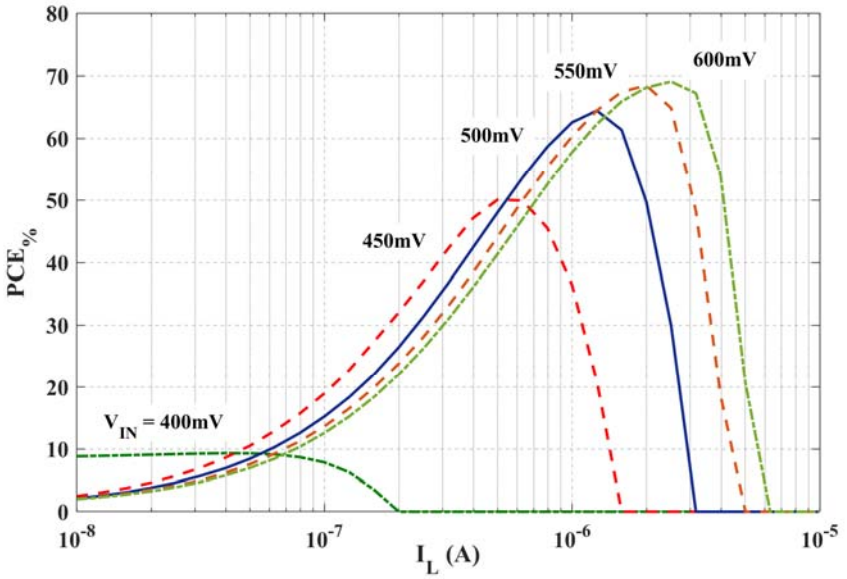


Voltage ripple factor = 0,62 mV/V

Simulation and measurement results



Simulated transient behaviour with current load



Measured power conversion efficiency as function of the current load for different values of the input voltage

Load Regulation = 3,97 mV/µA

Comparison with the State-of-the-Art

EXPERIMENTAL DATA SUMMARY AND COMPARISON WITH THE STATE-OF-THE-ART

	[17]	[16]	[9]	[8]	This Work
Technology	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS	0.13µm CMOS
Output regulation	yes	yes	no	yes	yes
Min.-Max. input voltage (V)	0.2-0.45	0.15-0.5	0.25-0.65	0.45-3	0.4-0.6
Output voltage (V)	1.3 (Unreg. 3.3)	0.85 (Unreg. 1.01)	3.8 - 4	3.3 (Unreg. NR)	1.25 (Unreg. 2.45)
Maximum voltage gain (V / V)	4	3	31	8	4.89
P_{OUT} range (µW)	0.1 - 10	NR	0 - 0.6	3.8 - 30.5	0 - 3
Peak efficiency (%) (Unreg.)	56 @ 2.41µW	67 @ 1.27µW	50 @ 8nW	72 @ 30µW	70 @ 3.75µW
Area (mm^2)	0.575	0.24	2.72	0.552	0.03
Power density (µW / mm^2)	4.19	5.29	0.0029	54.35	83.33

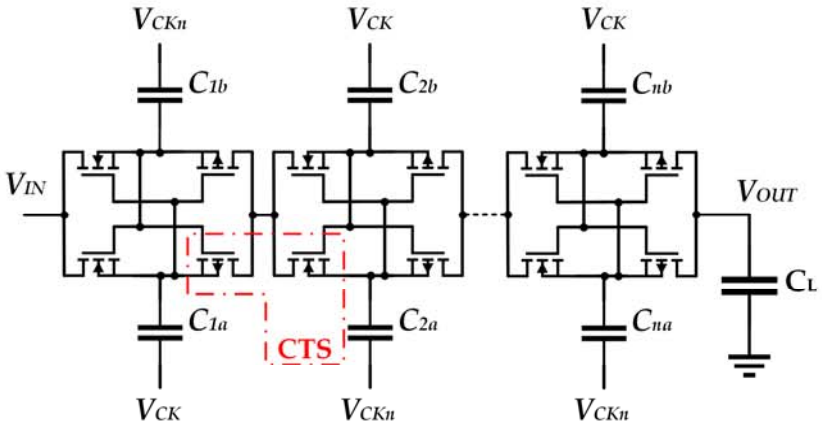
[8] X. Liu, L. Huang, K. Ravichandran, and E. Sánchez-Sinencio, "A highly efficient reconfigurable charge pump energy harvester with wide harvesting range and two-dimensional mppt for internet of things," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 5, pp. 1302–1312, 2016.

[9] X. Wu, Y. Shi, S. Jeloka, K. Yang, I. Lee, Y. Lee, D. Sylvester, and D. Blaauw, "A 20-pw discontinuous switched-capacitor energy harvester for smart sensor applications," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 4, pp. 972–984, 2017.

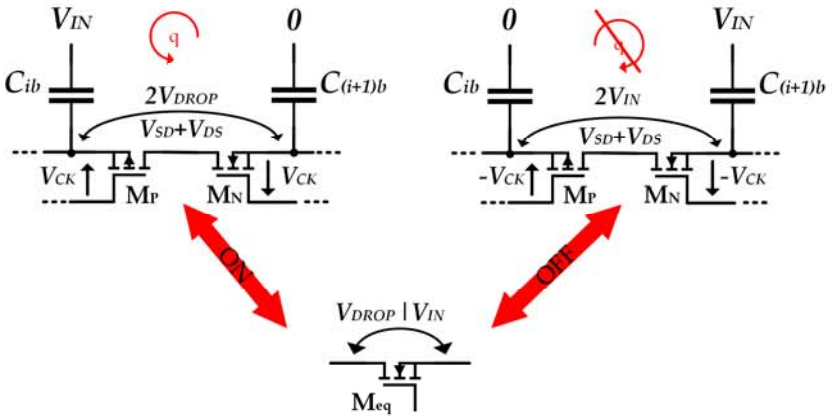
[16] Z. Chen, M.-K. Law, P.-I. Mak, and R. P. Martins, "A single-chip solar energy harvesting ic using integrated photodiodes for biomedical implant applications," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 11, no. 1, pp. 44–53, 2017.

[17] D. Cabello, E. Ferro, Pereira-Rial, B. Martinez-Vazquez, V. M. Brea, J. M. Carrillo, and P. Lopez, "On-chip solar energy harvester and pmu with cold start-up and regulated output voltage for biomedical applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 4, pp. 1103–1114, 2020.

Drawbacks in typically used topology



(a)



(b)

$$\frac{I_{FWD}}{I_{BWD}} \approx \frac{1-e^{-\frac{V_{DS,FWD}}{V_T}}}{1-e^{-\frac{V_{DS,BWD}}{V_T}}} e^{\frac{\Delta V_{GS}+\lambda_{DS}\Delta V_{DS}+\lambda_{BS}\Delta V_{BS}}{nV_T}}$$

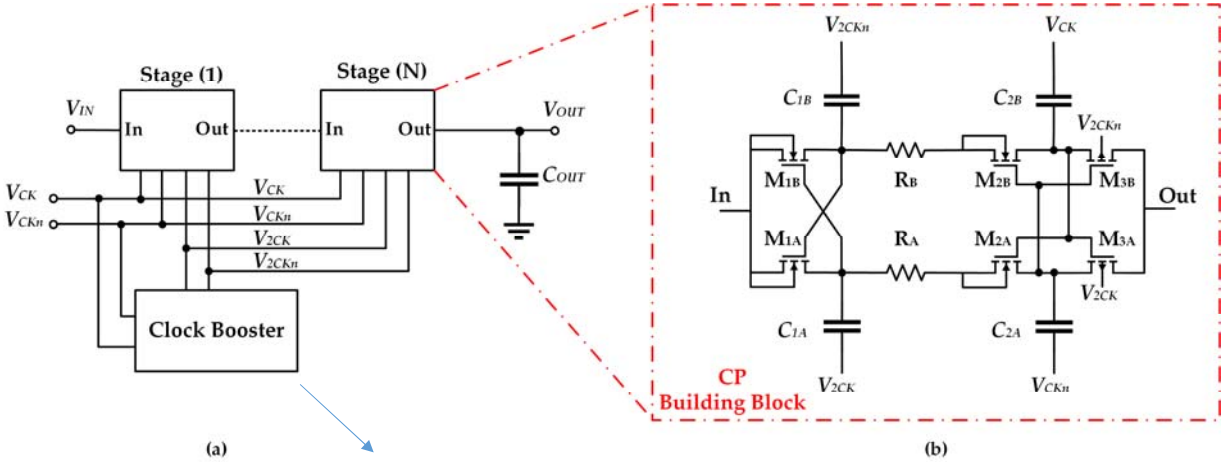
$$\left(V_{IN,\min}\right)_{cr-cpl} \approx \frac{\left(\Delta V_{GS}+\lambda_{BS,eq}\Delta V_{BS}\right)-nV_T\ln\left(\frac{V_T}{V_{DROP}}\right)}{\lambda_{DS,eq}}$$

Current driving capability is strongly reduced for very low voltage and this observable in the minimum input voltage

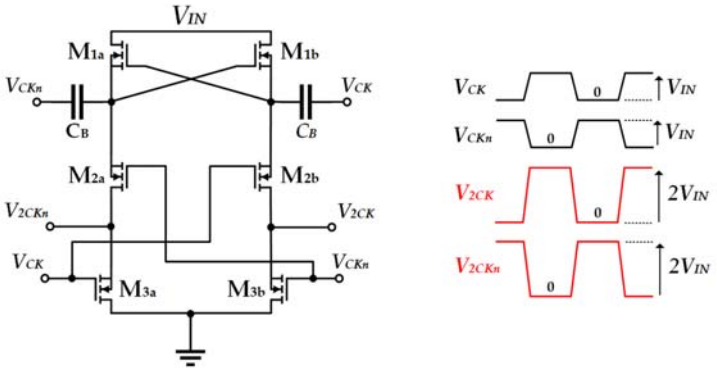
The proposed solution

We introduce a fully-integrated switched-capacitor DC-DC converter based on a Dickson charge pump

- **able to work with input voltage levels that force the transistors working in subthreshold region**
- **exploiting resistors in the charge transfer switch in order to overcome the limits of conventional solutions when working in the subthreshold regime.**

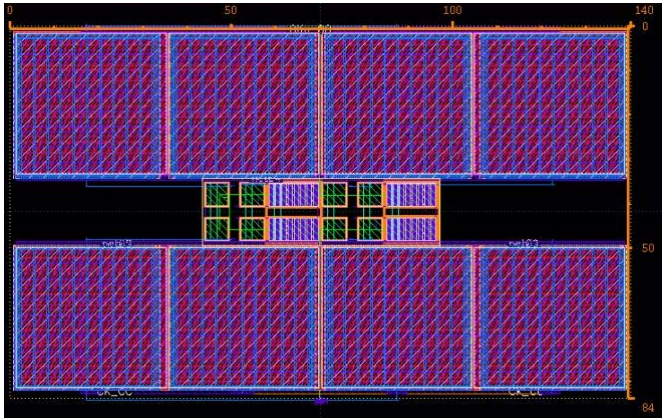


$$\left(V_{IN,\min}\right)_{proposed} \approx \frac{\left(\Delta V_{GS} + \lambda_{BS,n}\Delta V_{BS}\right) - nV_T \ln\left(\frac{V_T}{V_{DROP}}\right)}{3\lambda_{DS,n}}$$

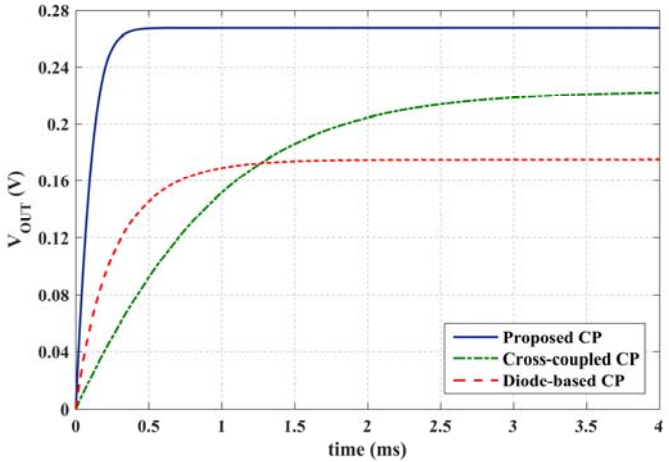


The minimum input voltage is lower than conventional cross-coupled CP

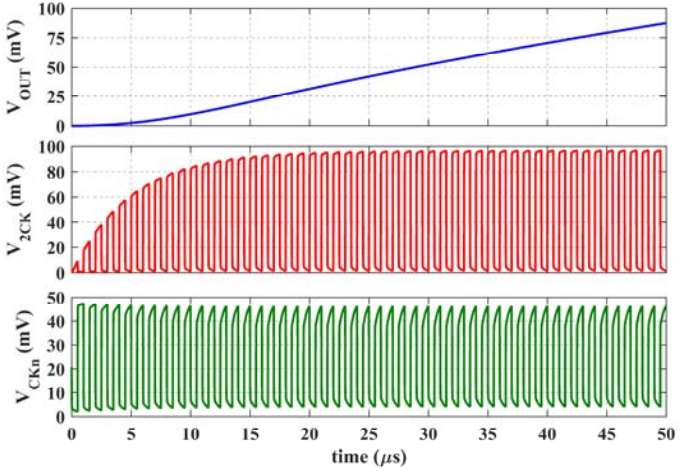
Simulation results



Layout of the charge pump

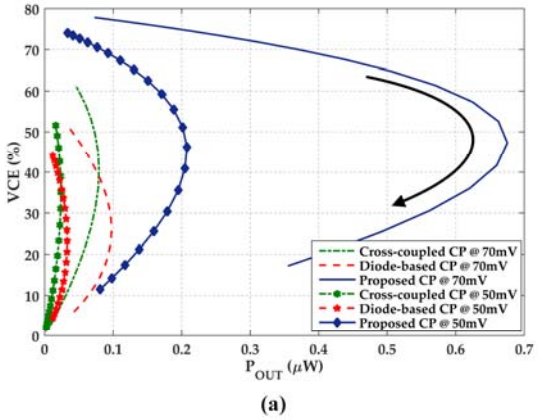


Simulated transient behaviours with only capacitive load

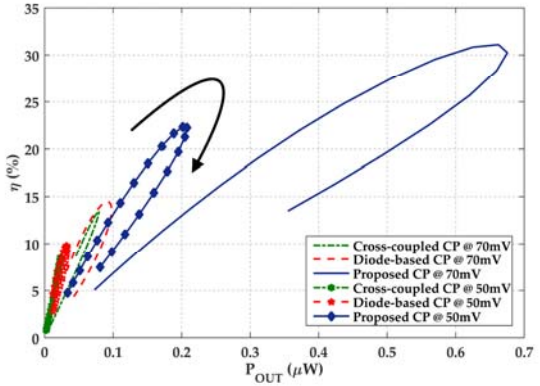


Simulation results

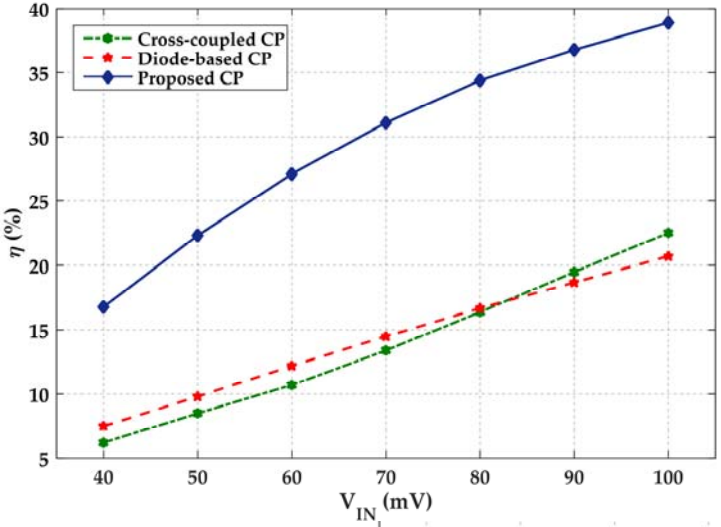
Voltage and Power Conversion Efficiency: Comparison

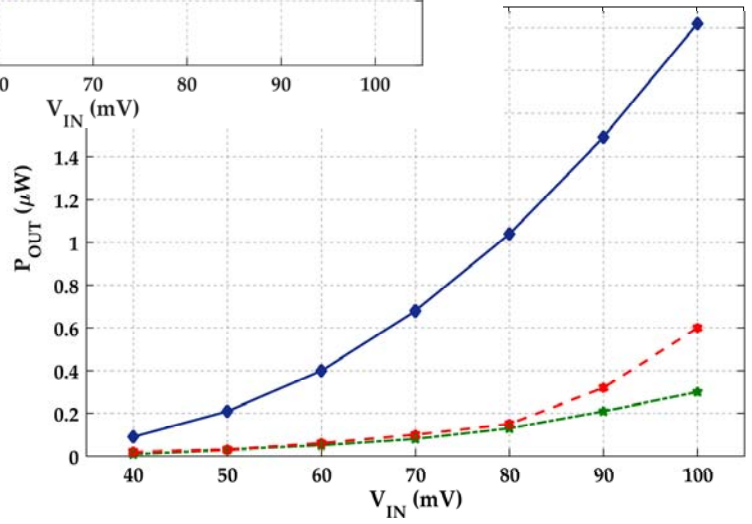


(a)



(b)

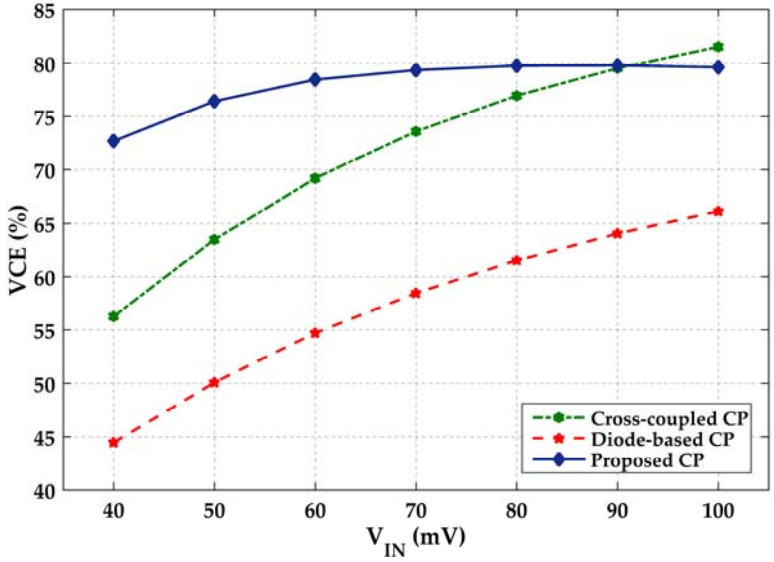




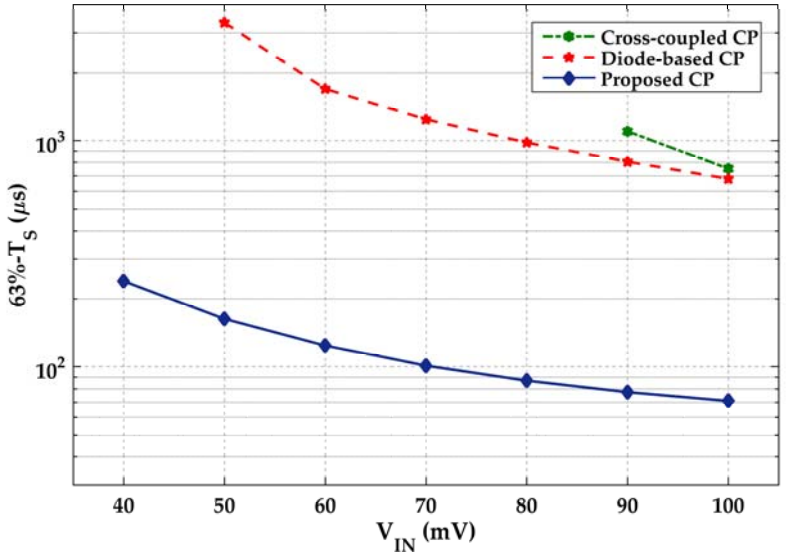
PCE and output power vs. input voltage

Simulation results

Voltage Conversion Efficiency vs. input voltage



Settling time vs. input voltage



THE PROPOSED SOLUTION IS MORE VOLTAGE EFFICIENT AND FASTER THAN THE CONVENTIONAL SOLUTIONS FOR LOWER INPUT VOLTAGES

Comparison with the State-of-the-Art

Ref.	Proposed [b]	[26]	[27]	[43]	[45]	[47]	[20]	[53]
Topology	Hybrid cross-coupled	Cross-coupled /composite	Cross-coupled	Bootstrap	Cross-coupled	Bootstrap	Cross-coupled	Adaptive
Technology (nm)	28	130	65	65	180	130	180	65
No. of stages	2	24	3	10	6	3	2x6	10
Auxiliary circuits	Clock booster 2x	Start-up circuit	Clock booster 3x	Clock booster 2x	Backward control circuit	--	Clock booster 2x	--
Application	TEG	TEG	TEG, solar cell	TEG, solar cell	TEG, solar cell	TEG, solar cell	TEG	TEG, solar cell
Minimum supply (mV)	50	70	150	100	320	270	57	120
Clock frequency (MHz)	1	0.040	15.2	10	0.45	0.8	0.025	1
Total pumping cap. (pF)	120	46.08	22.5	>1000	288	150	>1000	286
Load capacitance (pF)	180	10000 [a]	30	100	50.7	500	350	--
Settling time (s)	127	1.5 10^6	40	--	100	--	1.35 10^5	--
Max output power (μW)	0.68	15	1.5	6.6	--	7	0.08	3
Peak η (%)	38.9	58	38.8	33	78	58	89	38.8
Peak VCE (%)	80	50	80	76	89	58	93	58
Area (mm^2)	0.0116	0.6	0.032	1.32	1.37	0.42	0.96	0.78

[26] J. Goeppert and Y. Manoli, "Fully integrated startup at 70 mV of boost converters for thermoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 51, no. 7, pp. 1716–1726, Jul. 2016, doi: 10.1109/JSSC.2016.2563782.

[27] H. Yi, J. Yin, P.-I. Mak, and R. P. Martins, "A 0.032-mm^2 0.15-V three-stage charge-pump scheme using a differential bootstrapped ring-VCO for energy-harvesting applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 2, pp. 146–150, Feb. 2018, doi: 10.1109/TCSII.2017.2676159.

[43] H. Fuketa, S.-I. O'uchi, and T. Matsukawa, "Fully integrated, 100-mV minimum input voltage converter with gate-boosted charge pump kick-started by LC oscillator for energy harvesting," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 4, pp. 392–396, Apr. 2017, doi: 10.1109/TCSII.2016.2573382.

[45] H. Peng, N. Tang, Y. Yang, and D. Heo, "CMOS startup charge pump with body bias and backward control for energy harvesting step-up converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 6, pp. 1618–1628, Jun. 2014, doi: 10.1109/TCSI.2013.2290823.

[47] Y.-C. Shih and B. P. Otis, "An inductorless DC–DC converter for energy harvesting with a 1.2-μW bandgap-referenced output controller," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 58, no. 12, pp. 832–836, Dec. 2011, doi: 10.1109/TCSII.2011.2173967.

[20] S. Bose, T. Anand, and M. L. Johnston, "Integrated cold start of a boost converter at 57 mV using cross-coupled complementary charge pumps and ultra-low-voltage ring oscillator," *IEEE J. Solid-State Circuits*, vol. 54, no. 10, pp. 2867–2878, Oct. 2019, doi: 10.1109/JSSC.2019.2930911.

[53] P.-H. Chen, K. Ishida, X. Zhang, Y. Okuma, Y. Ryu, M. Takamiya, and T. Sakurai, "A 120-mV input, fully integrated dual-mode charge pump in 65-nm CMOS for thermoelectric energy harvester," in *Proc. 17th Asia South Pacific Design Autom. Conf.*, Jan. 2012, pp. 469–470, doi: 10.1109/ASPDAC.2012.6164994.

THE PROPOSED SOLUTION IS COMPACT AND FASTER AS COMPARED WITH PRIOR ART.

Q & A

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Thanks very much for your time and attention!

Questions/comments???