EnerHarv 2024

PSMA International Workshop | 26-28 June, 2024 | Perugia, Italy

Development of an Ultra-Low-Power Digital Energy-Harvesting PMIC platform

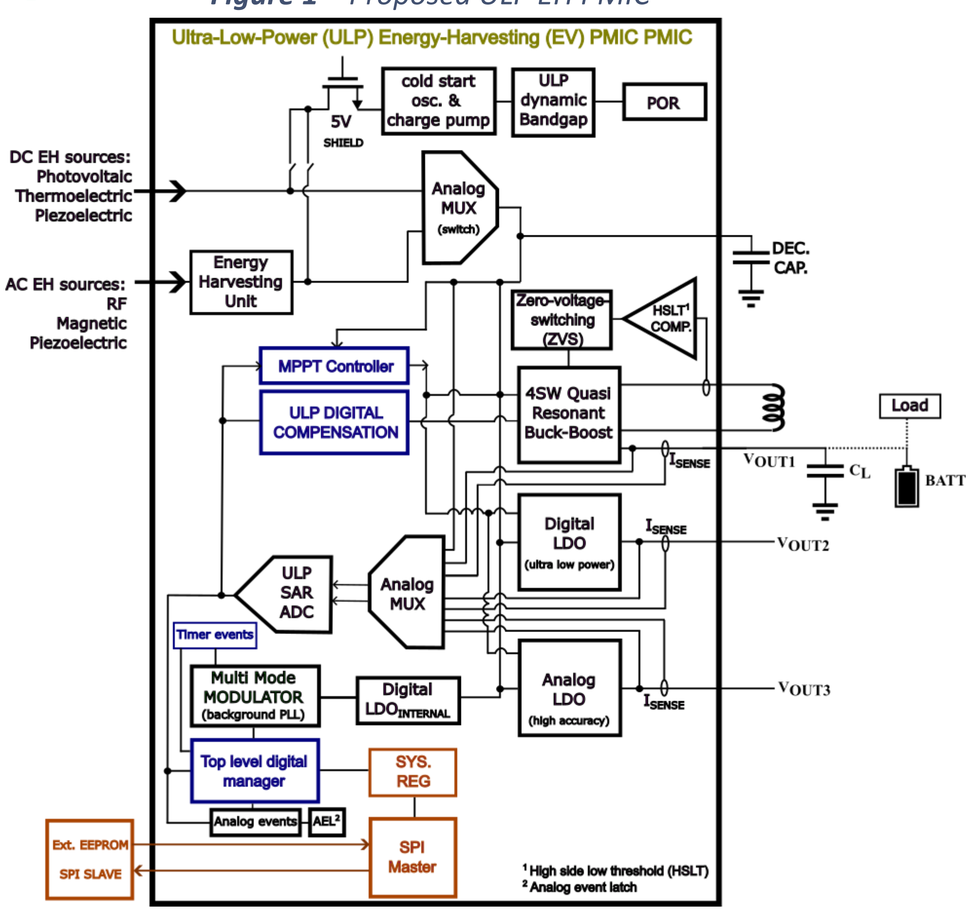
Hugo Cruz, Daniel Woodward, Seamus O'Driscoll, Mike Hayes,
Tyndall MCCI, hugo.cruz@tyndall.ie

ABSTRACT: An Energy Harvesting PMIC (EH-PMIC) platform under development is presented. Stand-by wake-up signals are pre-programmed with a 35-bit TDC. The main feature of the EH PMIC for ultra-low power is digitalization of most of the blocks, including the compensation of the switching converters. For high conversion efficiency from light-to-heavy current loads, retention mode, Pulse Frequency Modulation (PFM), and Pulse Width Modulation (PWM) are implemented, respectively. The converter switching efficiency is achieved in the 4-switch (4-SW) quasi resonant buck-boost converter by using a zero-voltage-switching (ZVS) technique.

Acknowledgement: This work was funded by EU Chips Act projects Energy ECS (#101007247) & LoLiPoP IoT (#101112286)

Block diagram

Figure 1 *– Proposed ULP EH PMIC*



Features

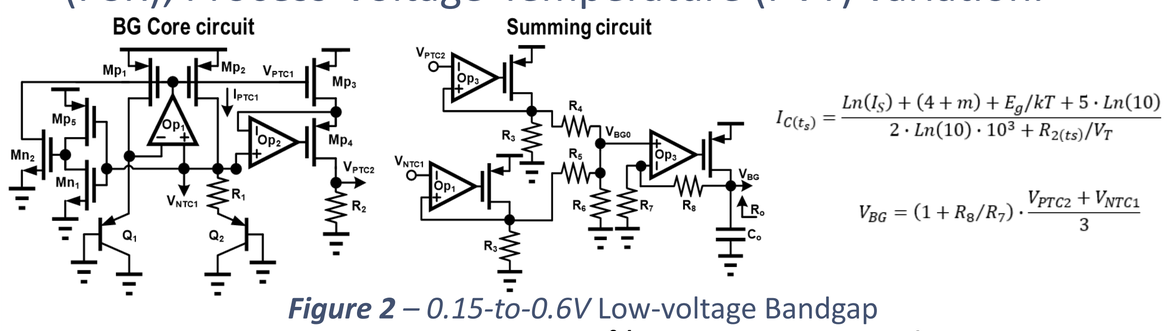
- Energy harvesting with Maximum-Power-Point-Tracking (MPPT)
- Digital 4-SW Quasi-resonant buck-boost w/i zero-voltage switch (ZVS) & High-side-low-threshold (HSLT) comparator for improved switching.
- Low-power 12-bit SAR ADC assisting Digital Controls.
- Converters in tri-mode operation: Retention mode, PFM, PWM for high efficiency through wide load range.
- Ultra-low-voltage cold start (200mV)

References

[1] Seamus O'Driscoll, "Ultra Low-Power PMIC Platform for Energy-Harvesting Smart Sensor for IoT," EnerHarv 2022.
[2] e-peas, "AEM13920 Dual input energy harvesting," doi: https://e-peas.com/product/aem13920-dual-source-energy-harvesting/
[3] Analog Devices Inc., analog.com , "ULTRALOW POWER VOLTAGE REGULATOR, SUPERVISORY, AND PMIC For Wireless Sensor Nodes, Wearable (Health Monitoring Access), and Cloud Connected Gateways," https://www.analog.com/media/en/news-marketing-collateral/solutions-bulletins-brochures/Ultralow-Power-Power-Management-Solution%20Brochure.pdf

Low voltage bandgap features:

- Current mirror with feedback converts I_{PTC1} into V_{PTC2}.
- Feedback purpose: improve Power-Supply-Rejection (PSR), Process-Voltage-Temperature (PVT) variation.



$$I_{C(t_s)} = \frac{Ln(I_S) + (4+m) + E_g/kT + 5 \cdot Ln(10)}{2 \cdot Ln(10) \cdot 10^3 + R_{2(ts)}/V_T}$$

$$V_{BG} = (1 + R_8/R_7) \cdot \frac{V_{PTC2} + V_{NTC1}}{3}$$

Figure 2 *– 0.15-to-0.6V* Low-voltage Bandgap

		[5]	[6]	[7]	[8]	[9]	[10]	This work
V_{BG}	DC (V)	< 0.8	0.585	1.0875	0.8	0.228	0.635	1.09, 0.6, 0.5, 0.45, 0.4, 0.35, 0.3, 0.25, 0.2, 0.15
	3σ (%)	14.1	3.66 (21.43 mV)[2]	±0.75 /0.15[3]	1.5 (12mV)	N/A	N/A	0.64(2.55 mV)
TC (ppm/°C)		41.5	110	12/42[3,4]MAX	60	34	<24.6 @VDD=1.5V	78.93 @ 1.2 V
Temp. (°C)		−40 to 85	−20 to 120	−40 to 125	−10 to 100	−40 to 120	5 to 95	−40 to 100
Turn-on time (us)		~100	>100	N/A	N/A	load trans. = 10 µs, ton ~ 22.8[5]	load trans. < 10 µs, ton ~ 31.75[5]	0.12
Load		N/A	N/A	N/A	N/A	9.6 mA max	1 mA, 100 pF	2 pF+18pF(probe)
Noise		N/A	N/A	6.1 uVRMS (0.1-10 Hz)	N/A	300 nV/√Hz @ 1kHz	N/A	61.98 nV/√Hz avg.: 1.96 mVRMS (integrated noise from 100-1GHz)
PSRR (dB)		N/A	−54 @ DC < −10 @ 100kHz	74 dB @ DC	N/A	−58 @ 100 Hz −12 @ 1 MHz	−47.6 @ 100 Hz < −10 @ 1 MHz	−33.72 @ 100 Hz, 25 °C −32.71 @ 1 MHz, 25 °C −21.5 @ 10 MHz, 25 °C
Supply (V)		1.425– 3.6	0.85–1.5	1.8	1.1	1–5	0.9–3.5	1.2–1.5
Area (mm²)		0.0094	0.0525	0.12	0.02	0.0464, 0.0445	0.059	0.0635
FOM[1]		0.367	0.577	N/A	N/A	1.07	1.45	3.35

[1]FOM=(1000·T_{ON}^{-1})/(TC·P·Area).

Table 1– Bandgap comparison table

High PSRR Analog Low-Dropout (LDO) regulator

Yun et al. 2017

Figure 4 *a) LDO with Tail-Current-Compensation (TTC) & Negative-Capacitance-Circuit(NCC), b) LDO with TTC, c) PSRR @ 2V, d) PSRR w/i & w/o NCC*

Figure 3 *a) VBG_0 and b) PSRR*

Summary
An Energy-Harvesting Power Management IC (EH PMIC) utilizing digitalization techniques that enables Ultra-Low-Power (ULP) is proposed. Digital filtering, control, and power stages are also digitalized to further reduce power consumption. For applications without high PSRR regulation, tri mode operation for buck/boost converters is used to enhance power conversion efficiency. Furthermore, for higher regulation and PSRR while maintaining low power, a Digital LDO is utilized. At the extreme, where highly linear regulation is required, a novel cap-less LDO with negative capacitance circuit (NCC) and Tail-Current Compensation (TCC) for 1uA to 100mA load is proposed.

ORGANISER

PSMA

HOST

A.D. 1308 unipg

MEDIA SPONSORS

HOW2POWER.COM

Bodo´s Power Systems®

COMMERCIAL SPONSORS

VITALITY

CONNECT Networks of the Future

WÜRTH ELEKTRONIK MORE THAN YOU EXPECT

Boston Scientific

e-peas semiconductors

EAGLE PROJECTS Technology Factory

TECHNICAL SPONSORS

pels IEEE POWER ELECTRONICS SOCIETY Powering a Sustainable Future

IEEE ELECTRONICS PACKAGING SOCIETY

UBIGIoT

LoLiPoP-IoT Energy Harvesting An EPSRC Funded Network

CPSS China Power Supply Society

SSIST

SFU SIMON FRASER UNIVERSITY ENGAGING THE WORLD